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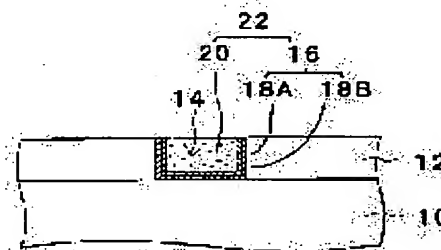
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**(54) WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE, FORMATION OF WIRING AND THIN SILVER FILM, CVD SYSTEM AND CHEMICAL/ MECHANICAL POLISHING METHOD**

(57)Abstract:

**PURPOSE:** To eliminate the patterning step for forming a wiring while solving the problems arising when an Al based alloy or Cu is employed as a wiring material.

**CONSTITUTION:** The wiring structure for a semiconductor device comprises (a). a trench 14 or an opening made in an insulation layer 12 formed on a substrate 10, and (b). a multilayer metal wiring layer 22 comprising a tight contact layer 16 and an Ag layer 20 formed in the trench 14 or the opening. The method for forming a wiring in a semiconductor device comprises a step for forming an insulation layer 12 on the substrate 10 and then making a trench 14 or an opening therein, a step for forming a multilayer metal wiring layer 22 comprising a tight contact layer 16 and an Ag layer 20 on the insulation film including the trench or the opening, and a step for removing the metal wiring layer 22 from above the insulation layer 12 while leaving the metal wiring layer 22 in the trench 14 or the opening.

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**CLAIMS**


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[Claim(s)]

[Claim 1] (b) the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer which were formed in the slot or opening formed in the insulating layer on a base, a (b) this slot, or opening circles -- since -- the wiring structure of the semiconductor device characterized by being constituted.

[Claim 2] Said adhesion layer is the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or the wiring structure of the semiconductor device according to claim 1 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom.

[Claim 3] Wiring structure of the semiconductor device according to claim 1 or 2 characterized by forming the sidewall which changes from SiN to the side attachment wall of said slot or opening.

[Claim 4] (b) the process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, and (\*\*) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer and Ag layer on the insulating layer containing this slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leave a metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by to change.

[Claim 5] formation of said Ag layer -- Ag<sub>2</sub> -- the wiring formation approach of the semiconductor device according to claim 4 characterized by being based on the chemistry gaseous-phase depositing method using CO<sub>3</sub>, AgNO<sub>2</sub>, AgBr, or AgI as a raw material.

[Claim 6] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 4 or 5 characterized by consisting of the chemical mechanical polish process of a metal wiring layer.

[Claim 7] The wiring formation approach of the semiconductor device according to claim 6 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I<sub>2</sub> and KI.

[Claim 8] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 4 or 5 characterized by consisting of the etchback process of a metal wiring layer.

[Claim 9] Said adhesion layer is the wiring formation approach of a semiconductor device given in any 1 term of the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer or claim 4 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom thru/or claim 8.

[Claim 10] The wiring formation approach of a semiconductor device given in any 1 term of claim 4 characterized by including further the process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 9.

[Claim 11] (b) the multilayer metal wiring layer which consists of the adhesion layer from the bottom formed in the slot or opening formed in the insulating layer on a base, a (b) this slot, or opening circles, Cu layer, and Ag layer -- since -- the wiring structure of the semiconductor device characterized by being constituted.

[Claim 12] Said adhesion layer is the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or the wiring structure of the semiconductor device according to claim 11 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom.

[Claim 13] Wiring structure of the semiconductor device according to claim 11 or 12 characterized by forming the sidewall which changes from SiN to the side attachment wall of said slot or opening.

[Claim 14] Wiring structure of the semiconductor device according to claim 11 or 12 characterized by forming the sidewall which changes from Ag to the side attachment wall of said slot or opening.

[Claim 15] (b) the process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, and (\*\*) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing this slot or opening circles, and the process which remove the metal wiring layer on an insulating layer (Ha), and leave a metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by to change.

[Claim 16] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 15 characterized by consisting of the chemical mechanical polish process of a metal wiring layer.

[Claim 17] The wiring formation approach of the semiconductor device according to claim 16 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I2 and KI.

[Claim 18] Removal of the metal wiring layer on the insulating layer in the process of the above (Ha) is the wiring formation approach of the semiconductor device according to claim 15 characterized by consisting of the etchback process of a metal wiring layer.

[Claim 19] (b) The process which forms a slot or opening in this insulating layer after forming an insulating layer on a base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) this slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- the wiring formation approach of the semiconductor device characterized by changing.

[Claim 20] Removal of the 1st metal wiring layer on the insulating layer in the process of the above (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of said (e) is the wiring formation approach of the semiconductor device according to claim 19 characterized by consisting of a chemical mechanical polish process.

[Claim 21] The wiring formation approach of the semiconductor device according to claim 20 characterized by performing the chemical mechanical polish of Ag layer using the mixed water solution of I2 and KI.

[Claim 22] Removal of the 1st metal wiring layer on the insulating layer in the process of the above (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of said (e) is the wiring formation approach of the semiconductor device according to claim 19 characterized by consisting of an etchback process.

[Claim 23] Said adhesion layer is the wiring formation approach of a semiconductor device given in any 1 term of the two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer or claim 15 characterized by consisting of the two-layer structure of Ag layer / Ti layer from the bottom thru/or claim 22.

[Claim 24] The wiring formation approach of a semiconductor device given in any 1 term of claim 15 characterized by including further the process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 23.

[Claim 25] The wiring formation approach of a semiconductor device given in any 1 term of claim

15 characterized by including further the process which forms the sidewall which changes from Ag to the side attachment wall of a slot or opening after the process of said (b) thru/or claim 23.

[Claim 26] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using  $\text{Ag}_2\text{CO}_3$  as a raw material.

[Claim 27] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using  $\text{AgNO}_2$  as a raw material.

[Claim 28] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using  $\text{AgBr}$  as a raw material.

[Claim 29] The formation approach of the silver thin film by the chemistry gaseous-phase depositing method using  $\text{AgI}$  as a raw material.

[Claim 30] The CVD system which is a CVD system equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber, and is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material.

[Claim 31] The 2nd heater is a CVD system according to claim 30 characterized by being lamp heating apparatus.

[Claim 32] The chemical mechanical polish method characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I2 and KI.

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DETAILED DESCRIPTION

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## [Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the CVD system suitable for formation of the wiring structure concerning the wiring structure of a semiconductor device where Ag (silver) was used as a wiring material and the wiring formation approach, the silver thin film formation approach, and a list, and the chemical mechanical polish method.

[0002]

[Description of the Prior Art] With high integration of a semiconductor device, the dimension of the manufacture process of a semiconductor device makes it detailed, and is also making detailed wiring width of face in a semiconductor device in connection with this. Pure aluminium or an aluminium alloy (hereafter, these are named generically and it is also called aluminum system alloy) is mainly used as current and a wiring material. And after, forming the metal wiring layer which consists of aluminum system alloy by the so-called elevated-temperature aluminum spatter method for example, on the substrate which consists of an insulating layer, this metal wiring layer is made into a desired pattern configuration with a photolithography technique and an etching technique. Of this, wiring which consists of aluminum system alloy is formed. Then, an insulator layer is formed on wiring and flattening processing of this insulator layer is performed.

[0003] In order to form a resist pattern with a photolithography technique on a metal wiring layer, it is necessary to stop the scattered reflection of the light by the metal wiring layer at the time of exposure. When the scattered reflection of light is not stopped at the time of exposure, halation arises under the effect of the scattered reflection of light, and the defect of the stage piece of a resist etc. arises in the formed resist pattern. Therefore, resist patterning is performed after usually forming the antireflection film which consists of TiON on a metal wiring layer.

[0004] Hereafter, the example of a manufacture process of the conventional semiconductor device based on the elevated-temperature aluminum spatter method and the flattening approach by polish is explained with reference to drawing 20, drawing 21, and drawing 22.

[0005] The component isolation region 102 and the gate field 104 are formed in the base 100 which consists of a [process -10] semi-conductor substrate. Then, a LDD ion implantation is performed, the gate sidewall 106 is formed, an ion implantation is performed and the source drain field 108 is formed (refer to (A) of drawing 20).

[0006] The layer insulation layer 112 is formed all over after that [ [process -20] ], and, subsequently to the layer insulation layer 112, opening 114 is formed (refer to (B) of drawing 20).

[0007] After forming the adhesion layer 116 which consists of Ti/TiN/Ti all over [a process -30], next the layer insulation layer 112 which contains opening 114 in a spatter, the metal wiring layer 118 which consists of aluminum system alloy (for example, aluminum-1wt%Si) by the elevated-temperature aluminum spatter method is made to deposit on the whole surface. Then, the antireflection film 120 which consists of TiON is formed in the whole surface. And wiring is formed by carrying out patterning of an antireflection film 120, the metal wiring layer 118, and the adhesion layer 116 with a photolithography technique and a dry etching technique (refer to

(C) of drawing 20 ).

[0008] [Process -40] Subsequently flattening processing by polish is performed. That is, the 1st insulator layer 122 which consists of SiO<sub>2</sub> by the plasma-CVD method all over the layer insulation layer 112 including wiring is formed, the stopper layer 124 which consists of SiN by the plasma-CVD method on it is formed, and the 2nd insulator layer 126 which consists of thick SiO<sub>2</sub> is further formed with a CVD method on it (refer to (A) of drawing 21 ).

[0009] The 2nd insulator layer 126 is ground from the upper part after that [ [process -50] ]. And it grinds until the stopper layer 124 appears as a polished surface (refer to (B) of drawing 21 ). In this way, the 1st insulator layer 122 by which flattening was carried out is formed after wiring.

[0010] Or the insulator layer by which flattening processing was carried out can also be formed at the following processes again instead of [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN.

[0011] The insulator layer 130 which consists of SiO<sub>2</sub> by the [process-40'] plasma-CVD method is formed.

[0012] After that [ [process-50'] ], a resist 132 is formed on an insulator layer 130, and patterning of the resist 132 is carried out so that the heights of an insulator layer 130 may be exposed (refer to (A) of drawing 22 ).

[0013] A resist 132 is removed after etching [process-60'], next the heights of an insulator layer 130 (refer to (B) of drawing 22 ).

[0014] a part of insulator layer 130 which remained after that [ [process-70'] ], without being etched -- 130A is ground and flattening of an insulator layer 130 is performed.

[0015]

[Problem(s) to be Solved by the Invention] If wiring makes it detailed, it will become difficult to form the wiring width of face made into the purpose with a sufficient controllability. In response to the effect of the irregularity of the layer insulation layer 112 which is a substrate, irregularity arises in the front face of the metal wiring layer 118. Moreover, it is easy to be ruined when the metal wiring layer 118 which consists of aluminum system alloy is formed by the elevated-temperature aluminum spatter method etc. (that is, irregularity is easy to be formed). It originates in these and the coverage of the antireflection film 120 in the crevice of the metal wiring layer 118 falls (for example, refer to (C) of drawing 20 ). In order for the reflection factor of the light in the part to fall, the scattered reflection of light arises, and it becomes impossible consequently, to form the target patterning configuration to the metal wiring layer 118 under the effect of halation etc. as a result.

[0016] Moreover, the wiring structure after resist patterning is the 120/metal wiring layer 118 of antireflection films which consists of a top to TiON. Dry etching performs patterning of the metal wiring layer 118 after resist patterning. In this case, BCl<sub>3</sub> system gas is usually used as etching gas. However, etching by BCl<sub>3</sub> system gas is only a chemical reaction, and it is impossible to etch the antireflection film 120 which consists of TiON by BCl<sub>3</sub> system gas. So, it is necessary to etch the antireflection film 120 in a physical spatter operation.

[0017] Therefore, in case the metal wiring layer 118 which consists of aluminum system alloy is etched, it is necessary to change into chemical etching conditions from the etching conditions which have a spatter operation. However, when the thickness of the 120/metal wiring layer 118 of antireflection film is uneven, these etching serves as an ununiformity by modification of such etching conditions.

[0018] Furthermore, the approach explained at [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN has the following troubles. That is, although the stopper layer 124 is used in case the 2nd insulator layer 126 which consists of SiO<sub>2</sub> is ground, the selection ratio to polish of SiO<sub>2</sub> and SiN is obtained three to about six. Therefore, it does not function as a stopper so that the stopper layer 124 which consists of SiN may perform the terminal point judging of polish, but the 1st insulator layer 122 may be ground too much. Namely, the 2nd insulator layer 126 cannot be ground with a sufficient controllability. Consequently, it has the problem that perfect flattening of the 1st insulator layer 122 cannot be attained.

[0019] And if spacing of wiring is thin in case between wiring is embedded by the 1st insulator

layer 122 which consists of SiO<sub>2</sub> or SOG with a CVD method etc., the embedding of the 1st insulator layer 122 becomes inadequate, and it also has the problem that "\*\* (void)" 122A occurs in the 1st insulator layer 122 during wiring (refer to drawing 23 ).

[0020] on the other hand -- SiN -- from -- changing -- a stopper -- a layer -- 124 -- not using -- [ -- a process - 40 -- ' -- ] - [ -- a process - 70 -- ' -- ] -- having explained -- an approach -- also setting -- an insulator layer -- 130 -- polish -- the time -- an insulator layer -- 130 -- polish -- a terminal point -- a judgment -- carrying out -- \*\*\*\* . For this reason, it has the problem of grinding an insulator layer 130 too much.

[0021] Thus, in manufacture of a detailed semiconductor device, after forming wiring, the conventional approach of forming a flat insulator layer on it has the above various troubles, and there is still no approach for solving these troubles effectively.

[0022] In the above-mentioned process, aluminum system alloy is used as a wiring material. In the metal wiring layer 118 which consists of aluminum system alloy, electromigration is a big problem. Moreover, at the time of the dry etching of the metal wiring layer 118, by the corrosion of a metal wiring layer, a void occurs in a metal wiring layer and the dependability fall of wiring is caused. As a result of the aluminum particle in the metal wiring layer 118 moving when a current is passed to wiring as detailed wiring-ization progresses especially, current concentration arises in the minute chip void generated in the metal wiring layer. Therefore, it was missing with electromigration and much more dependability fall of wiring is caused by compound operation of a void.

[0023] Using copper (Cu) as a wiring material as a way stage which solves this problem is proposed. However, there is no suitable etching approach of Cu and it has various problems -- that the workability of Cu is not good, and heat treatment in the furnace which contains oxygen several% that it is very easy to oxidize cannot be performed. The problem of workability forms a slot in an insulating layer, and after making Cu deposit on an insulating layer including this slot, it can avoid it by grinding Cu on an insulating layer chemically and mechanically by the chemical mechanical polish method. However, an effective means to prevent oxidation of the front face of Cu embedded in the slot is not known.

[0024] Therefore, the 1st purpose of this invention does not need to perform the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring. and the insulating layer which includes wiring, without grinding the insulator layer formed on wiring like before -- completeness -- it is in offering the wiring structure and the wiring formation approach of a new semiconductor device which make flattening possible and can solve the trouble at the time of using aluminum system alloy and Cu as a wiring material further.

[0025] The 2nd purpose of this invention is to offer the new silver thin film formation approach. Furthermore, the 3rd purpose of this invention is to provide the CVD system list suitable for application to this wiring structure and the wiring formation approach with the chemical mechanical polish method.

[0026]

[Means for Solving the Problem] the 1st voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles -- since -- it is characterized by being constituted.

[0027] In the wiring structure of the semiconductor device concerning the 1st mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, in order to prevent oxidation of a metal wiring layer on the side attachment wall of a slot or opening, the sidewall which consists of SiN may be formed.

[0028] The wiring formation approach of the semiconductor device concerning the 1st mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (\*\*) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion



layer and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0029] the 1st voice of this invention -- the wiring formation approach of the semiconductor device applied like -- setting -- formation of Ag layer -- Ag<sub>2</sub> -- it can carry out by the chemistry gaseous-phase depositing method using CO<sub>3</sub>, AgNO<sub>2</sub>, AgBr, or AgI as a raw material. Removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of a chemical mechanical polish process of a metal wiring layer, or an etchback process of a metal wiring layer. the chemical mechanical polish method -- setting -- the mixed water solution of I<sub>2</sub> and KI -- using -- the chemical mechanical polish of Ag layer -- it can carry out.

[0030] Moreover, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. The process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of (b) can be included further.

[0031] the 2nd voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles, Cu layer, and Ag layer -- since -- it is characterized by being constituted.

[0032] In the wiring structure of the semiconductor device concerning the 2nd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, SiN or the sidewall which consists of Ag again may be formed in the side attachment wall of a slot or opening.

[0033] The wiring formation approach of the semiconductor device concerning the 2nd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (\*\*) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0034] In the wiring formation approach of the semiconductor device concerning the 2nd mode of this invention, removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of chemical mechanical polish processes of a metal wiring layer. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I<sub>2</sub> and KI. Or removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of etchback processes of a metal wiring layer again.

[0035] The wiring formation approach of the semiconductor device concerning the 3rd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0036] the 3rd voice of this invention -- in the wiring formation approach of the semiconductor device applied like, removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of chemical mechanical polish processes. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I<sub>2</sub> and KI. Or removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of etchback processes

again.

[0037] In the wiring formation approach of the semiconductor device concerning the 2nd or 3rd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, the process which forms the sidewall which changes from SiN or Ag to the side attachment wall of a slot or opening after the process of (b) can be included further.

[0038] The formation approach of the silver thin film for attaining the 2nd above-mentioned purpose is characterized by depending Ag<sub>2</sub>CO<sub>3</sub> on the chemistry gaseous-phase depositing method used as a raw material. Or it is characterized by being based on the chemistry gaseous-phase depositing method using AgNO<sub>2</sub> as a raw material again. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgBr as a raw material. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using AgI as a raw material. These raw materials are gasified and it uses as CVD gas using carrier gas, such as inert gas.

[0039] The CVD system of this invention for attaining the 3rd above-mentioned purpose is equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber. And it is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater can be used as lamp heating apparatus.

[0040] The chemical mechanical polish method for attaining the 3rd above-mentioned purpose is characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I<sub>2</sub> and KI.

[0041]

[Function] The metal wiring layer is formed in a slot or opening circles in this invention. Such a metal wiring layer of a gestalt removes the metal wiring layer on an insulating layer, and since it is formed by leaving a metal wiring layer to a slot or opening circles, it does not need to perform patterning of the metal wiring layer formed on the insulating layer by the photolithography technique and the dry etching technique like the conventional technique. Moreover, since flattening processing by removal of the metal wiring layer on an insulating layer is performed, it is not necessary to perform flattening processing of the insulator layer formed on wiring like a Prior art.

[0042] Ag cannot oxidize easily due to elevated-temperature heat treatment. Although Ag also oxidizes, it decomposes into AgO→Ag+O at the temperature more than 100-degreeC. For this reason, AgO is not stable at the temperature of hundreds of degreeC, and the oxide of Ag is not maintained. Moreover, since a metal wiring layer is constituted from Ag, the problem of electromigration like aluminum system alloy is not generated. Therefore, stable wiring can be formed in the wiring structure or the wiring formation approach concerning the 1st mode of this invention.

[0043] In the wiring formation approach concerning the wiring structure or the 2nd or 3rd mode concerning the 2nd mode of this invention, since a metal wiring layer is constituted from an Ag layer and a Cu layer, the problem of electromigration like aluminum system alloy is not generated. And since the front face of Cu layer is covered with Ag layer, oxidation of Cu layer can be prevented.

[0044] Hereafter, with reference to a drawing, this invention is explained based on an example. In addition, in an example 1 – an example 6, the wiring formation approach concerning the wiring structure and the 1st mode of a semiconductor device concerning the 1st mode of this invention is explained. Moreover, in an example 7 – an example 12, the wiring formation approach concerning the wiring structure and the 2nd mode of a semiconductor device concerning the 2nd mode of this invention is explained. Furthermore, in an example 13 – an example 15, the wiring formation approach concerning the wiring structure and the 3rd mode of a semiconductor device concerning the 2nd mode of this invention is explained.

[0045] (Example 1) an example 1 – an example 6 -- the 1st voice of this invention -- the wiring structure of the semiconductor device applied like, and the 1st voice -- it is related with the

wiring formation approach which starts like. The wiring structure of an example 1 changes from the multilayer metal wiring layer 22 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 1 so that a sectional view may be shown in part. The metal wiring layer 22 consists of an adhesion layer 16 and an Ag layer 20 from the bottom. The adhesion layer 16 is the two-layer structure of Ti layer 18 A/TiN layer 18B from the bottom.

[0046] the wiring formation approach of an example 1 -- (\*\*) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (\*\*) -- it consists of the process which forms from the bottom the multilayer metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and the process which remove the metal wiring layer 22 on an insulating layer (Ha) 12, and leave the metal wiring layer 22 in a slot 14 on an insulating layer 12 including the inside of a slot 14. Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used  $\text{Ag}_2\text{CO}_3$  as a raw material. Moreover, removal of the metal wiring layer 22 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 22 of having used the mixed water solution of I2 and KI. By operating as a stopper the insulating layer 12 which consists of  $\text{SiO}_2$ , it becomes possible to set up the selection ratio of the metal wiring layer 22 and insulating layer 12 to a chemical mechanical polish to infinity.

[0047] Hereafter, with reference to typical drawing 2 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 1 is explained concretely.

[0048] The insulating layer 12 which consists of  $\text{SiO}_2$  is formed on the base 10 which consists of [a process -100, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be carried out as follows.

Gas used :  $\text{SiH}_4/\text{O}_2/\text{N}_2=250/250 / 100\text{sccm}$  substrate heating temperature: 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0049] A slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique after that [ [process -110] ] (refer to (A) of drawing 2 ). In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 2 . The conditions of dry etching can be carried out as follows.

Gas used :  $\text{C}_4\text{F}_8=50\text{sccm}$  RF power : 1200W pressure : 2Pa [0050] The adhesion layer 16 which consists of Ti layer 18 A/TiN layer 18B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -120] next (refer to (B) of drawing 2 ). The adhesion layer 16 can be formed on condition that the following.

Formation use gas 150 degreeC thickness of Ti layer 18A :  $\text{Ar}=100\text{sccm}$  power : 4kW pressure : 0.47Pa membrane formation temperature : : Formation use gas of 50nmTiN layer 18B :

$\text{Ar}/\text{N}_2=40/70\text{sccm}$  power : 5kW pressure : 0.47Pa thickness : 70nm [0051] The silver (Ag) layer 20 is formed in the whole surface with a CVD method after that [ [process -130] ] (refer to (C) of drawing 2 ). Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used  $\text{Ag}_2\text{CO}_3$  as a raw material. The conditions of CVD can be carried out as follows.

Raw material : Source temperature of  $\text{Ag}_2\text{CO}_3$  raw material : 170-degreeC use gas :  $\text{Ag}_2\text{CO}_3/\text{Ar}/\text{H}_2=10/25/1000\text{sccm}$  pressure :  $2.6 \times 10^3\text{Pa}$  substrate heating temperature: By this, the Ag layer 20 deposits on the 450-degreeC insulating layer 12 including the inside of a slot 14. The Ag layer 20 is formed of the following reaction.

$\text{Ag}_2\text{CO}_3+\text{H}_2 \rightarrow 2\text{Ag}+\text{CO}_2+\text{H}_2\text{O}$  [0052] The CVD system of this invention shown in drawing 3 for formation of the Ag layer 20 was used. This CVD system is equipped with the piping 204 which connects the CVD chamber 200, the source 202 of a raw material, the source of a raw material, and a CVD chamber. And it has the 1st heater 206 which heats piping 204 more than the boiling point of a raw material, and the 2nd heater 210 which heats the CVD chamber induction 208 for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater 210 is lamp heating apparatus, and the mirror 212 is formed.

Moreover, the aperture 214 made from a quartz is formed in the part of the about 208 CVD chamber induction [ which opposes the 2nd heater 210 ] piping 204. In addition, it is a heater for lamp heating apparatus for 216 to heat a base 10 and 218 to heat inert gas induction among drawing 3 , and for 220 heat the source 202 of a raw material. At the 1st and 2nd heaters

206,210, Ag<sub>2</sub>CO<sub>3</sub> gas which flows the inside of piping 204 and the CVD chamber induction 208 is held more than 218-degreeC which is the boiling point.

[0053] By [a process -140], next the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 20 and the adhesion layer 16, and wiring which consists of the metal wiring layer 22 is formed (refer to drawing 1 ). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.

Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x108Pa pad temperature : A chemical mechanical polish is performed using the mixed water solution of 40 degreeC I<sub>2</sub>+KI.

[0054] since a slurry (abrasive material +KOH+ water of SiO<sub>2</sub> system) is used when grinding SiO<sub>2</sub> conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO<sub>2</sub> is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 20 and the adhesion layer 16, a slurry is not needed, but by grinding with the mixed water solution of I<sub>2</sub>+KI, it is possible to remove only the Ag layer 20 and the adhesion layer 16, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.

[0055] Wiring which consists of the metal wiring layer 22 embedded at the flat insulating layer 12 by this is formed. In an example 1, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.

[0056] (Example 2) In the example 1, the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 22 is removed [ in / instead / an example 2 ] by the etchback method by dry etching. In addition, other processes are the same as an example 1, and detailed explanation is omitted.

[0057] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20 in a slot 14 for the Ag layer 20 and the adhesion layer 16 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 22] slot 14.

Gas used : NO<sub>2</sub>/O<sub>2</sub>=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100-degreeC

[0058] (Example 3) In an example 3, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -110] of an example 1 and [a process -120] is included further. In addition, other processes are the same as an example 1, and detailed explanation is omitted.

Hereafter, the formation process of the sidewall 26 of an example 3 is explained with reference to drawing 5 . By forming a sidewall 26, oxidation of the adhesion layer 16 by the insulating layer 12 can be prevented.

[0059] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 5 ). The formation conditions of SiN layer 26A are illustrated below.

Gas used: SiH<sub>4</sub>/NH<sub>3</sub>/N<sub>2</sub>=180/500/720sccm temperature : 200-degreeC pressure : 40Pa thickness : 100nm

[0060] Then, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 5 ). The conditions of etchback can be carried out as follows.

Gas used : CHF<sub>3</sub>=50sccmRF power : 300W pressure : 2Pa of sidewalls 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 5 can be formed through [process -120] - [a process -140]. [ of an example 1 ]

[0061] (Example 4) The wiring structure of an example 4 typical to drawing 6 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 1 and a little and consists of a semi-conductor substrate, It consists of metal

wiring layers 22 which consist of the adhesion layer 16 and the Ag layer 20 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 24 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 22.

[0062] The wiring formation approaches of an example 4 differ an example 1 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and form wiring structure. The metal wiring layer 22 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 4 is explained with reference to typical drawing 7 and typical drawing 8 which are sectional views a part, such as a semiconductor device.

[0063] On the base 10 which consists of the semi-conductor substrate which consists of. [Process] -400 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, in order to form the gate sidewall 34 in the whole surface, SiO<sub>2</sub> film is made to deposit, after performing a LDD ion implantation. The deposition conditions of SiO<sub>2</sub> film can be carried out as follows.

Gas used : SiH<sub>4</sub>/O<sub>2</sub>-/N<sub>2</sub>=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : Further, whole surface etchback of SiO<sub>2</sub> film is performed and 0.25 micrometers of gate sidewalls 34 are formed in the side attachment wall of the gate field 32. Whole surface etchback can be performed on condition that the following.

Gas used : C<sub>4</sub>F<sub>8</sub>=50sccmRF power: 1200W pressure : An impurity ion implantation is performed on condition that the following after that [ 2Pa ] for formation of the source drain field 36. formation As of an N type channel Formation BF 2 of 20KeV and 5x10<sup>15</sup>-/cm<sup>2</sup> P type channel 20KeV and 3x10<sup>15</sup>-/cm<sup>2</sup> -- a part typical to (A) of drawing 7 in this way -- the structure shown with a sectional view can be acquired.

[0064] 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with the CVD method of the following conditions after that [ [process -410] ]. SiO two-layer formation use gas : TEOS 50sccm pressure : 40Pa temperature : 720-degreeC thickness : Formation use gas of 400nmBPSG layers : SiH<sub>4</sub>/PH<sub>3</sub>/B-2H<sub>6</sub>/O<sub>2</sub>/N<sub>2</sub>=80/7/7/1000/32000sccm temperature : 400-degreeC pressure : 1.0x10<sup>5</sup>Pa thickness : 500nm 900 more degreeC and reflow processing for 20 minutes are performed, and flattening of 1st insulating-layer 12A is performed.

[0065] [A process -420], next 2nd insulating-layer 12B which consists of SiO<sub>2</sub> are formed in the whole surface. 2nd insulating-layer 12B can be formed on condition that the following.

Gas used : SiH<sub>4</sub>/O<sub>2</sub>-/N<sub>2</sub>=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa

thickness : 0.8 micrometers [0066] Slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -110] of an example 1 after that [ [process -430] ] (refer to (B) of drawing 7 ).

[0067] [Process -440] Subsequently opening 14A is formed in 1st insulating-layer 12A by performing dry etching after resist patterning (refer to (C) of drawing 7 ). Here, width of face of slot 14B is made larger than the path of opening 14A. The conditions of dry etching can be carried out as follows.

Gas used : C<sub>4</sub>F<sub>8</sub> 50sccmRF power: 1200W pressure : Further, 2Pa of 1100-degreeC and activation annealing for 10 seconds are performed, after forming a junction field by performing an ion implantation to opening circles. The following examples can be given as conditions for an ion implantation.

Formation As of an N type channel Formation BF 2 of 20KeV and 5x10<sup>15</sup>-/cm<sup>2</sup> P type channel 20KeV, 3x10<sup>15</sup>-/cm<sup>2</sup> [0068] It is desirable to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer subsequently like [the formation process of a sidewall 26] of an example 3, and to form the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the side attachment wall of

slot 14B after that [ [process -450] ], (refer to (A) of drawing 8 ).

[0069] The adhesion layer 16 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -460] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.

[0070] The Ag layer 20 is formed in the whole surface like the [process -130] of an example 1 after that [ [process -470] ] by the chemistry gaseous-phase depositing method using  $\text{Ag}_2\text{CO}_3$  as a raw material (refer to (B) of drawing 8 ).

[0071] Like [a process -480], next the [process -140] of an example 1, by the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 20 and the adhesion layer 16, and the connection hole and wiring which consist of the metal wiring layer 22 are formed (refer to drawing 6 ). That is, the connection hole (for example, the so-called contact hole) with which the metal wiring layer 22 was embedded is formed in opening 14A. Moreover, the wiring 24 with which the metal wiring layer 22 was embedded at slot 14B is formed.

[0072] In addition, it is also removable by carrying out etchback by the dry etching method like an example 2 instead of removing the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 by the chemical mechanical polish method.

[0073] (Example 5) An example 5 is deformation of an example 4. Although the wiring structure of an example 5 is the same as an example 4, the wiring formation approach is different from an example 4. That is, opening 14A prepared in 1st insulating-layer 12A is embedded with the metal wiring material which consists of Ag, connection hole 24A is completed, subsequently to a it top, 2nd insulating-layer 12B is made to deposit, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 4. In an example 5, [the process -400], [a process -410], and [a process -440] of an example 4 are same process, and other processes differ. Hereafter, the approach of an example 5 is explained with reference to drawing 9 and drawing 10 .

[0074]

On the base 10 which consists of the semi-conductor substrate of [process -500] -[process -520] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for formation of the source drain field 36. Then, 1st insulating-layer 12A which consists of two-layer [ of  $\text{SiO}_2$  and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after resist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -400] of an example 4, [a process -410], and [a process -440]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.

[0075] [Process -530]

1st adhesion layer 16A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -520] by the same approach as the [process -120] of an example 1.

Subsequently, by the same approach as the [process -130] of an example 1, 1st Ag layer 20A is formed on the whole surface with a CVD method, and the 1st metal wiring layer which consists of 1st adhesion layer 16A and 1st Ag layer 20A is formed (refer to (A) of drawing 9 ).

[0076] After that [ [process -540] ], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 20A and 16A only in opening 14A (refer to (B) of drawing 9 ). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1. Of this, the so-called contact hole 24A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 20A and 16A only in opening 14A with the etchback by the dry etching method like an example 2.



[0077] [Process -550] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -420] of an example 4. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -430] of an example 4 (refer to (A) of drawing 10). Then, if needed, a SiN layer may be formed in the whole surface by the plasma-CVD method, subsequently whole surface etchback of the SiN layer may be carried out like the [process -450] of an example 4, and the sidewall (not shown) which changes from SiN to the side attachment wall of slot 14B by this may be formed.

[0078] By the same approach as [a process -560], next the [process -120] of an example 1 After forming in a spatter 2nd adhesion layer 16B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1 2nd Ag layer 20B is formed on the whole surface with a CVD method, and the 2nd metal wiring layer which consists of 2nd adhesion layer 16B and 2nd Ag layer 20B is formed.

[0079] [Process -570] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves 2nd Ag layer 20B and 2nd adhesion layer 16B, and wiring 24 is formed (refer to (B) of drawing 10). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1.

[0080] In addition, instead of removing the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B by the chemical mechanical polish method, like an example 2, etchback of the 2nd metal wiring layer 20B and 16B is carried out by the dry etching method, it can leave the 2nd metal wiring layer 20B and 16B only in slot 14B, and wiring 24 can also be formed in slot 14B by this.

[0081] (Example 6) An example 6 is deformation of an example 5. The point that an example 6 is different from an example 5 is in the point which forms a tungsten plug with a CVD method in opening 14A beforehand. Hereafter, the wiring formation approach of an example 6 is explained with reference to drawing 11.

[0082]

[Process -600] - [a process -620] These processes can be made to be the same as that of [process -500] - [a process -520]. [ of an example 5 ]

[0083] [Process -630]

The barrier layer 40 which consists of Ti/TiN is formed in the whole surface in a spatter after [a process -620], and the tungsten layer 42 is formed with a CVD method all over after that (refer to (A) of drawing 11). The membrane formation conditions of Ti and TiN can be made to be the same as that of the [process -120] of an example 1. Moreover, the membrane formation conditions of the tungsten by the CVD method are illustrated below.

Gas used : WF<sub>6</sub>/H<sub>2</sub>=95 / 550sccm membrane formation temperature : 450-degreeC pressure :

1.1x10<sup>4</sup>Pa thickness : 0.4 micrometers [0084] After that [ [process -640] ], etchback is performed by the dry etching method, the tungsten layer 42 and the barrier layer 40 on 1st insulating-layer 12A are removed, and it leaves the metal plug and the barrier layer 40 which consist of the tungsten layer 42 only in opening 14A (refer to (B) of drawing 11). The conditions of dry etching can be carried out as follows.

Gas used : SF<sub>6</sub>=50sccm microwave power: 850WRF power : 150W pressure : Contact hole 24A which consists of the so-called tungsten plug by which the tungsten was embedded at opening 14A by this 1.33Pa is formed. In addition, it may leave the tungsten layer 42 and the barrier layer 40 only in opening 14A by the chemical mechanical polish method instead of the etchback by the dry etching method.

[0085] [Process -650] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -550] of an example 5. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -550] of an example 5. In addition, width of face of slot 14B is made larger than the path of opening 14A.

[0086] After forming in a spatter the adhesion layer 16 which consists of Ti of 30nm thickness by the same approach as [a process -660], next the [process -560] of an example 5 on 2nd

insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1, the Ag layer 20 is formed on the whole surface with a CVD method, and the metal wiring layer which consists of the adhesion layer 16 and the Ag layer 20 is formed.

[0087] The metal wiring layer on 2nd insulating-layer 12B is removed with the etchback by the chemical mechanical polish method or dry etching after that [ [process -670] ] by the same approach as the [process -140] of an example 1. By this, it leaves a metal wiring layer only in slot 14B, and the wiring 24 which consisted of metal wiring layers which consist of the adhesion layer 16 and the Ag layer 20 in slot 14B is formed (refer to (C) of drawing 11 ).

[0088] (Example 7) an example 7 -- an example 12 -- the 2nd voice of this invention -- the wiring structure of the semiconductor device applied like, and the 2nd voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 7 changes from the multilayer metal wiring layer 50 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 12 so that a sectional view may be shown in part. The metal wiring layer 50 consists of an adhesion layer 52, a Cu layer 54, and an Ag layer 56 from the bottom. Moreover, the adhesion layer 52 is the two-layer structure of Ti layer 52 A/TiN layer 52B from the bottom.

[0089] the wiring formation approach of an example 7 -- (\*\*)-- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (\*\*)-- it consists on an insulating layer 12 including a slot 14 of the process which forms from the bottom the multilayer metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and the process which removes the metal wiring layer 50 on an insulating layer (Ha) 12, and leaves a metal wiring layer in a slot 14.

[0090] Formation of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 is performed in a spatter. Moreover, removal of the metal wiring layer 50 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 50. By operating as a stopper the insulating layer 12 which consists of SiO<sub>2</sub>, it becomes possible to set up the selection ratio of the metal wiring layer 50 and insulating layer 12 to a chemical mechanical polish to infinity.

[0091] Hereafter, with reference to typical drawing 13 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 7 is explained concretely.

[0092] The insulating layer 12 which consists of SiO<sub>2</sub> is formed on the base 10 which consists of [a process -700, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 13 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.

[0093] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -710] next (refer to (A) of drawing 13 ). The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.

[0094] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [ [process -720] ] (refer to (B) of drawing 13 ). The Cu layer 54 can be formed on the following spatter conditions.

Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 500nm [0095] The silver (Ag) layer 56 is formed in the whole surface in a spatter after that [ [process -730] ] (refer to (C) of drawing 13 ). The Ag layer 56 can be formed in the spatter of the following conditions.

Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nm of front faces of the Cu layer 54 is covered with the Ag layer 56 in this way.

[0096] By [a process -740], next the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 56, the Cu layer 54, and the



adhesion layer 52, and wiring which consists of the metal wiring layer 50 is formed (refer to drawing 12 ). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.

Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force :  $5.5 \times 10^8 \text{Pa}$  pad temperature : The mixed water solution of  $\text{I}_2 + \text{KI}$  is used for removal by the chemical mechanical polish method of the 40-degreeC Ag layer 56. Moreover,  $\text{K}_4\text{Fe}(\text{CN})_6 + \text{H}_2\text{O}$  is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.

[0097] since a slurry (abrasive material +KOH+ water of  $\text{SiO}_2$  system) is used when grinding  $\text{SiO}_2$  conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case  $\text{SiO}_2$  is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 56, the Cu layer 54, and the adhesion layer 52, a slurry is not needed, but by grinding in the mixed water solution of  $\text{I}_2 + \text{KI}$ , and  $\text{K}_4\text{Fe}(\text{CN})_6$  water solution, it is possible to remove only the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.

[0098] Wiring which consists of the metal wiring layer 50 embedded at the flat insulating layer 12 by this is formed. In an example 7, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.

[0099] (Example 8) In the example 7, the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 50 is removed [ in / instead / an example 2 ] by the etchback method by dry etching. In addition, other processes are the same as an example 7, and detailed explanation is omitted.

[0100] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 in a slot 14 for the Ag layer 56, the Cu layer 54, and the adhesion layer 52 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 50] slot 14. The etching use gas of the Ag layer 56 :  $\text{NO}_2/\text{O}_2=20 / 20\text{sccm}$  microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : Etching use gas of the 100-degreeCCu layer 54 and the adhesion layer 52 :  $\text{O}_2-\text{Cl}_2=10 / 70\text{sccm}$  microwave power: 1000WRF power : 300W pressure : 0.5Pa substrate heating temperature : 300-degreeC [0101]

(Example 9) In an example 9, the process which forms the sidewall 26 which changes from  $\text{SiN}$  to the side attachment wall of a slot 14 between the [process -710] of an example 7 and [a process -720] is included further. In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 9 is explained with reference to drawing 14 . By forming a sidewall 26, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.

[0102]  $\text{SiN}$  layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 14 ). Next, whole surface etchback of the  $\text{SiN}$  layer 26A is carried out (refer to (B) of drawing 14 ). The formation conditions of  $\text{SiN}$  layer 26A and the conditions of etchback can be made to be the same as that of an example 3. A sidewall 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 14 can be formed through [process -720] - [a process -740]. [ of an example 7 ]

[0103] (Example 10) The sidewall 26 which consists of  $\text{SiN}$  in an example 9 was formed in the side attachment wall of a slot 14. On the other hand, in an example 10, a sidewall is formed from Ag (silver). In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall of an example 10 is explained. By forming the sidewall which consists of Ag, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.

[0104] Ag layer is made to deposit in a spatter the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall which consists of Ag] slot 14. Next, whole surface etchback of the Ag layer is carried out. The formation conditions of Ag layer and the conditions of etchback are illustrated below.

Ag stratification condition use gas : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nmAg layer etchback condition use gas : NO<sub>2</sub>/O<sub>2</sub>=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100degreeC -- the same sidewall can be formed in the side attachment wall of a slot 14 with having been shown in drawing 14 in this way. Henceforth, the same wiring structure can be formed with having been shown in (C) of drawing 14 through [process -720] - [a process -740]. [ of an example 7 ]

[0105] (Example 11) The wiring structure of an example 11 typical to drawing 15 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 7 and a little and consists of a semi-conductor substrate. It consists of metal wiring layers 50 which consist of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 58 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 50.

[0106] The wiring formation approaches of an example 11 differ an example 7 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and form wiring structure. The metal wiring layer 50 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 11 is explained with reference to typical drawing 16 which is sectional views a part, such as a semiconductor device.

[0107] On the base 10 which consists of the semi-conductor substrate of [Process] -1100 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation.

[0108] After that [ [process -1110] ], 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed.

[0109] [Process -1120] Subsequently to a 1st insulating-layer 12A top, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed.

[0110] Slot 14B is formed in 2nd insulating-layer 12B after that [ [process -1130] ].

[0111] [Process -1140] Opening 14A is further formed in 1st insulating-layer 12A. Subsequently, activation annealing is performed after making a junction field form by performing an ion implantation to opening circles.

[0112] The above process can be made to be the same as that of [process -400] - [a process -440]. [ of an example 4 ]

[0113] [Process -1150] Subsequently the sidewall 26 which consists of SiN may be formed in the side attachment wall of opening 14A and slot 14B like the [process -450] of an example 4. Of the above process, the structure shown in (A) of drawing 16 is formed.

[0114] The adhesion layer 52 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -1160] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.

[0115] The Cu layer 54 is formed in the whole surface in a spatter like the [process -720] of an example 7 after that [ [process -1170] ]. Subsequently, the Ag layer 56 is formed in the whole surface in a spatter like the [process -730] of an example 7 (refer to (B) of drawing 16 ).

[0116] After that [ [process -1180] ], like the [process -740] of an example 7, by the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on 2nd

insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and the connection hole and wiring which consist of the metal wiring layer 50 are formed (refer to drawing 15 ). That is, connection hole 58A (for example, the so-called contact hole) where the metal wiring layer 50 was embedded is formed in opening 14A. Moreover, the wiring 58 with which the metal wiring layer 50 was embedded at slot 14B is formed.

[0117] In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 by the chemical mechanical polish method.

[0118] (Example 12) An example 12 is deformation of an example 11. Although the wiring structure of an example 12 is the same as an example 11, the wiring formation approach is different from an example 11. That is, after embedding opening 14A prepared in 1st insulating-layer 12A with the metal wiring material which consists of Cu and completing connection hole 58A, 2nd insulating-layer 12B is made to deposit on it, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 11. In an example 12, [the process -1100], [a process -1110], and [a process -1140] of an example 11 are same process, and other processes differ. Hereafter, the approach of an example 12 is explained with reference to drawing 17 .

[0119]

On the base 10 which consists of the semi-conductor substrate of [process -1200] -[process -1220] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation. Then, 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after resist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -1100] of an example 4, [a process -1110], and [a process -1140]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.

[0120] [Process -1230]

1st adhesion layer 52A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -1220] by the same approach as the [process -710] of an example 7. Subsequently, by the same approach as the [process -720] of an example 7, 1st Cu layer 54A is formed on the whole surface in a spatter, and the 1st metal wiring layer which consists of 1st adhesion layer 52A and 1st Cu layer 54A is formed.

[0121] After that [ [process -1240] ], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 54A and 52A only in opening 14A (refer to (A) of drawing 17 ). The conditions of a chemical mechanical polish can be made to be the same as that of the chemical mechanical polish of Cu layer of the [process -740] of an example 7. Of this, the so-called contact hole 58A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 54A and 52A only in opening 14A with the etchback by the dry etching method like an example 8.

[0122] [Process -1250] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -1120] of an example 11. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -1130] of an example 11. Then, subsequently it can form and be easy to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer, and to have the sidewall (not shown) which consists of SiN in the side attachment wall of slot 14B by this if needed, like the [process -1150] of an example 11.

[0123] By the same approach as [a process -1260], next the [process -710] of an example 7

After forming in a spatter 2nd adhesion layer 52B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -730] of an example 7. The 2nd metal wiring layer which consists of 2nd adhesion layer 52B, 2nd Cu layer 54B, and the Ag layer 56 is formed by forming 2nd Cu layer 54B on the whole surface in a spatter, and forming the Ag layer 56 in a spatter on it further.

[0124] [Process -1270] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves the Ag layer 56, Cu layer of \*\* 2nd 54B, and 2nd adhesion layer 52B, and wiring 58 is formed (refer to (B) of drawing 18 ). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -740] of an example 7.

[0125] In addition, instead of removing the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B by the chemical mechanical polish method Like an example 8, etchback of the 2nd metal wiring layer 56, 54B, and 52B is carried out by the dry etching method, by this, it can leave the 2nd metal wiring layer 56, 54B, and 52B only in slot 14B, and wiring 58 can also be formed in slot 14B.

[0126] (Example 13) an example 7 - an example 12 -- setting -- the wiring structure of a semiconductor device -- the 2nd voice of this invention -- it formed by the wiring formation approach which starts like. On the other hand, the wiring structure of the semiconductor device in an example 13 - an example 15 is formed by the wiring formation approach concerning the 3rd mode of this invention.

[0127] The process which forms a slot 14 in an insulating layer 12 after the wiring formation approach of the semiconductor device of an example 13 forms an insulating layer 12 on the (b) base 10. The process which forms from the bottom 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 on the insulating layer 12 including the (b) slot 14. The process which removes 1st metal wiring layer 50A on an insulating layer 12, and leaves 1st metal wiring layer 50A in a slot 14, (Ha) It consists of the process which forms 2nd metal wiring layer 50B which consists of Ag layer on the (d) insulating layer 12 and 1st metal wiring layer 50A, and the process which removes 2nd metal wiring layer 50B on the (e) insulating layer 12, and leaves 2nd metal wiring layer 50B in a slot 14.

[0128] The adhesion layer 52, the Cu layer 54, and formation at metal wiring layer 50B to the 2nd are performed in a spatter. Moreover, removal of 2nd metal wiring layer 50B on the insulating layer 12 in the process of (e) changes from the chemical mechanical polish process of the metal wiring layer 50 to removal of 1st metal wiring layer 50A on the insulating layer 12 in the process of (Ha), and a list. By operating as a stopper the insulating layer 12 which consists of SiO<sub>2</sub>, it becomes possible to set up the selection ratio of the 1st [ to a chemical mechanical polish ], and 2nd metal wiring layers 50A and 50B, and an insulating layer 12 to infinity.

[0129] In the wiring formation approach concerning the 3rd mode of this invention, the Cu layer 54 can be covered with 2nd metal wiring layer 50B which consists of Ag layer much more more certainly than the wiring formation approach concerning the 2nd mode of this invention.

[0130] Hereafter, with reference to typical drawing 18 and typical drawing 19 which are sectional views a part, such as a semiconductor device, the wiring formation approach of an example 13 is explained concretely.

[0131] The insulating layer 12 which consists of SiO<sub>2</sub> is formed on the base 10 which consists of [a process -1300, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 18 . The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.

[0132] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -1310] next. The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.

[0133] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [ [process -1320] ] (refer to (A) of drawing 18 ). Formation of the Cu layer 54 can be made to be the same

as that of the [process -720] of an example 7. In this way, 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 can be formed from the bottom on the insulating layer 12 including a slot 14.

[0134] By [a process -1330], next the chemical mechanical polish method, the Cu layer 54 and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, and it leaves 1st metal wiring layer 50A which consists of the Cu layer 54 and the adhesion layer 52 in a slot 14 (refer to (B) of drawing 18 ). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be made to be the same as that of an example 13.  $K_4Fe(CN)_6 + H_2O$  is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.

[0135] 2nd metal wiring layer 50B which consists of a silver (Ag) layer is formed in the whole surface in a spatter after that [ [process -1340] ] (refer to (A) of drawing 19 ). Formation of Ag layer can be made to be the same as that of the [process -730] of an example 13. In this way, the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B which consists of Ag layer.

[0136] By [a process -1350], next the chemical mechanical polish method, 2nd metal wiring layer 50B which consists of Ag layer on an insulating layer 12 is ground chemically and mechanically, and is removed, it leaves 2nd metal wiring layer 50B which consists of Ag layer in a slot 14, and wiring which consists of the 1st and 2nd metal wiring layers 50A and 50B is formed (refer to (B) of drawing 19 ). The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. In addition, the mixed water solution of  $I_2 + KI$  is used for removal by the chemical mechanical polish method of Ag layer.

[0137] In an example 13, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary. Moreover, since the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B much more certainly, oxidation of the Cu layer 54 which constitutes 1st metal wiring layer 50A can be prevented.

[0138] In an example 13, although 1st metal wiring layer 50A and 2nd metal wiring layer 50B were chiefly removed by the chemical mechanical polish method, it is also removable like an example 8 with the etchback by the dry etching method.

[0139] Moreover, formation of the sidewall explained in the wiring formation approach, and the example 9 or example 10 of the semiconductor device concerning the 3rd mode of this invention explained in the example 13 is also combinable. Furthermore, the wiring formation approach explained in the example 13 is also applicable instead of the Ag layer 56 in an example 11 or an example 12.

[0140] (Example 14) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 11 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0141] Formation of the component isolation region to a [process -1400] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.

[Process -1410] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [ of  $SiO_2$  and BPSG ].

[Process -1420] Formation of the 2nd insulating layer which consists of  $SiO_2$  to a 1st insulating-layer top.

Formation of the slot to the 2nd insulating layer of [a process -1430].

Formation of opening to the 1st insulating layer of [a process -1440].

Formation by the spatter to a 2nd insulating-layer top including opening and the slot of an adhesion layer which consist of a [process -1450] Ti layer / TiN layer.

Formation of Cu layer by the spatter to a [process -1460] adhesion layer top.

Removal of Cu layer on the 2nd insulating layer by the [process -1470] chemical mechanical polish.

Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1470] surface.

Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1480] chemical mechanical polish method.

[0142] (Example 15) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 12 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0143] Formation of the component isolation region to a [process -1500] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.

[Process -1510] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [ of SiO<sub>2</sub> and BPSG ].

Formation of opening to the 1st insulating layer of [a process -1520].

[Process -1530] Formation by the spatter of the 1st metal wiring layer which consists of the 1st adhesion layer to a 1st insulating-layer top, and 1st Cu layer.

Removal of the 1st metal wiring layer on the 1st insulating layer by the [process -1540] chemical mechanical polish method. By this, the so-called contact hole where the 1st metal wiring layer was embedded at opening is formed.

Formation of the 2nd insulating layer which consists of SiO<sub>2</sub> all over [a process -1550].

Formation of the slot to the 2nd insulating layer.

[Process -1560] Formation by the spatter of the 2nd adhesion layer to a 2nd insulating-layer top, and Cu layer.

Removal of Cu layer on the 2nd insulating layer by the [process -1570] chemical mechanical polish, and the 2nd adhesion layer.

Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1580] surface.

Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1590] chemical mechanical polish method.

[0144] As mentioned above, although this invention was explained based on the desirable example, this invention is not limited to these examples. The various ingredients and the conditions of having used in the example are instantiation, and can be changed suitably. Depending on the case, opening can be formed instead of Slots 14 and 14B.

[0145] Although the insulating layer was explained as what consists of the combination of SiO<sub>2</sub> or SiO<sub>2</sub>, and BPSG chiefly, it can constitute from what carried out the laminating of well-known insulating materials, such as BPSG, PSG and BSG, AsSG, PbSG, SbSG, SOG, SiON, or SiN, or these insulating layers to instead of [ these ].

[0146] In an example 1 - an example 6, although formation of the Ag layer 20 was performed by the chemistry gaseous-phase depositing method for having used Ag<sub>2</sub>CO<sub>3</sub> as a raw material instead, it can be performed by the chemistry gaseous-phase depositing method using AgNO<sub>2</sub>, AgBr, or AgI as a raw material. The CVD conditions in these cases and the heating conditions of the material gas which flows the inside of piping 204 and the CVD chamber induction 208 at the 1st and 2nd heaters 206,210 in the CVD system shown in drawing 3 are illustrated and combined with below, and a reaction formula is shown.

[0147] raw material: -- source temperature of AgNO<sub>2</sub> raw material 450-degreeC gas heating condition: -- more than 140-degreeC -- reaction-formula :  $2\text{AgNO}_2 + 7\text{H}_2 -$

$>2\text{Ag} + 2\text{NH}_3 + 4\text{H}_2\text{O}$  : 150-degreeC use gas : AgNO<sub>2</sub>/Ar/H<sub>2</sub>=10/25/1000sccm pressure :

2.6x10<sup>3</sup>Pa substrate heating temperature : [0148] Raw material: Source temperature of an AgBr raw material : 450-degreeC use gas : AgBr/Ar/H<sub>2</sub>=10/75 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa

substrate heating temperature: 500-degreeC gas heating conditions: It is power more than 434-degreeC. : 500W (plasma CVD).



Reaction formula :  $2\text{AgBr} + \text{H}_2 \rightarrow 2\text{Ag} + 2\text{HBr}$  \*\* [0149] Raw material: Source temperature of an AgI raw material : 560-degreeC use gas : AgI/Ar/H<sub>2</sub>=10/100 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature: 600-degreeC gas heating conditions: It is power more than 552-degreeC. : 500W (plasma CVD)

Reaction formula :  $2\text{AgI} + \text{H}_2 \rightarrow 2\text{Ag} + 2\text{HI}$  \*\* [0150] In an example 7 - an example 15, it can form with a CVD method instead of forming Cu layer and/or Ag layer in a spatter. The formation conditions of Cu layer by the CVD method are illustrated below.

Gas used : Cu (HFA)<sub>2</sub>/H<sub>2</sub>=10 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature: 350-degreeC power : It is the abbreviation for hexafluoro acetylacetonate in 500W, in addition HFA.

[0151] An adhesion layer can also consist of a Ti layer or a TiN layer instead of Ti layer / TiN layer. The formation conditions of the Ti layer or the TiN layer in this case can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1, and TiN layer 18B. Or an adhesion layer can also be made into the two-layer structure of Ag layer / Ti layer from the bottom again. In this case, Ag layer can be formed in the spatter of the following conditions. Moreover, the formation conditions of Ti layer can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1.

Spatter condition use gas of Ag layer : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 50nm [0152] TiON and TiW can also be used instead of TiN which constitutes an adhesion layer. Moreover, by the case, the sequence of formation of a slot, formation of a sidewall, and formation of an adhesion layer can be changed, and it can also consider as the order of formation of a slot, formation of an adhesion layer, and formation of a sidewall. Moreover, the metal layer or metallic-compounds layer which constitutes adhesion layers, such as Ti and TiN, can be formed by the forming-membranes methods, such as CVD.

[0153] The silicon layer formed on the various substrates for producing the various component sections, such as an insulating layer in which the MgO substrate, the GaAs substrate, superconducting transistor substrate, and lower layer wiring layer other than a silicon semiconductor substrate or the semi-conductor substrate with which the source drain field was formed were formed as a base, and a gate electrode which needs to form a connection hole ( a contact hole, a beer hall, through hole), and needs to form electrical installation, and a thin film transistor can be mentioned.

[0154] In an example 6, although the tungsten plug was formed in opening 14A using the so-called blanket tungsten CVD method, a tungsten plug may be instead formed in opening 14A with the so-called tungsten selection CVD method. The conditions in this case can be carried out as follows. Gas used : WF<sub>6</sub>/SiH<sub>4</sub>/H<sub>2</sub>/Ar=10/7/1000/10 sccm \*\* Whenever : 260-degreeC \*\* Force : 26Pa [0155] This invention is applicable to other semiconductor devices other than an MOS semiconductor device (for example, a bipolar transistor, CCD).

[0156] Various kinds of sputtering systems, such as a magnetron sputtering system, DC sputtering system, RF sputtering system, an ECR sputtering system, and a bias sputtering system that impresses substrate bias, can perform a spatter.

[0157] In the wiring structure concerning the 1st mode of this invention under Ag layer again the 2nd voice of this invention -- the wiring structure which starts like -- setting -- the bottom of Cu layer -- or -- again -- the wiring layer or connection hole under an adhesion layer -- refractory metals, such as Mo and Ti, -- Or a monolayer or various combination \*\*\*\*\* can be formed for the silicide of TiW, ZrN, W, WC, TiC, other MoSi<sub>2</sub> and WSi<sub>2</sub>, and TiSi<sub>2</sub> grade etc.

[0158]

[Effect of the Invention] In this invention, the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring is unnecessary. Therefore, the scattered reflection of the light in the conventional photolithography technique, or the heterogeneity of etching and the problem of a corrosion in dry etching is avoidable.

[0159] Moreover, in production of a semiconductor device which has detailed wiring, flattening with a perfect insulating layer including wiring becomes possible, without performing formation of

the insulator layer formed on wiring like before, or polish of this insulator layer. since the conventional SiO<sub>2</sub> system insulator layer was deficient in the selectivity in polish, the controllability of polish was scarce, but since the selectivity over an insulating layer is large, the controllability of polish is also boiled markedly and polish's of a metal wiring layer improves.

[0160] Furthermore, in order to leave a metal wiring layer only to a slot or opening circles, by adopting the etchback by the chemical mechanical polish method or the dry etching method, a Prior art can be used as it is fundamentally, and the manufacturing cost of a semiconductor device does not increase.

[0161] In addition, by forming a sidewall in a slot or opening circles, oxidation of a metal wiring layer can be prevented, moreover, by the metal wiring layer, it is stabilized and a slot or opening can be embedded.

[0162] In the wiring structure and the wiring formation approach concerning the 1st mode of this invention, since wiring structure is constituted from an Ag layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Furthermore, since resistance is lower than aluminum system alloy, Ag can expect the response speed of a semiconductor device.

[0163] In the wiring formation approach which starts the wiring structure concerning the 2nd mode of this invention, and a list at the 2nd and 3rd modes, since a metal wiring layer is constituted from a Cu layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Moreover, since the front face of Cu layer is covered with Ag layer, while preventing oxidation of Cu layer, wiring resistance can be kept low with the low resistance of Ag. Although Cu had the need for process limitation on problems, such as oxidation, conventionally, it becomes possible to use processes, such as heat treatment of an oxygen ambient atmosphere.

[0164] By the silver thin film formation approach of this invention, CVD of Ag becomes possible and the perfect embedding of Ag to a slot or opening becomes possible.

[0165] Furthermore, in the CVD system of this invention, since the source charging line to a CVD chamber and the connection of a CVD chamber can be held to high temperature, it is stabilized and material gas can be supplied.

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[Translation done.]



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**TECHNICAL FIELD**

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[Industrial Application] This invention relates to the CVD system suitable for formation of the wiring structure concerning the wiring structure of a semiconductor device where Ag (silver) was used as a wiring material and the wiring formation approach, the silver thin film formation approach, and a list, and the chemical mechanical polish method.

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[Translation done.]

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PRIOR ART

[Description of the Prior Art] With high integration of a semiconductor device, the dimension of the manufacture process of a semiconductor device makes it detailed, and is also making detailed wiring width of face in a semiconductor device in connection with this. Pure aluminium or an aluminium alloy (hereafter, these are named generically and it is also called aluminum system alloy) is mainly used as current and a wiring material. And after, forming the metal wiring layer which consists of aluminum system alloy by the so-called elevated-temperature aluminum spatter method for example, on the substrate which consists of an insulating layer, this metal wiring layer is made into a desired pattern configuration with a photolithography technique and an etching technique. Of this, wiring which consists of aluminum system alloy is formed. Then, an insulator layer is formed on wiring and flattening processing of this insulator layer is performed.

[0003] In order to form a resist pattern with a photolithography technique on a metal wiring layer, it is necessary to stop the scattered reflection of the light by the metal wiring layer at the time of exposure. When the scattered reflection of light is not stopped at the time of exposure, halation arises under the effect of the scattered reflection of light, and the defect of the stage piece of a resist etc. arises in the formed resist pattern. Therefore, resist patterning is performed after usually forming the antireflection film which consists of TiON on a metal wiring layer.

[0004] Hereafter, the example of a manufacture process of the conventional semiconductor device based on the elevated-temperature aluminum spatter method and the flattening approach by polish is explained with reference to drawing 20, drawing 21, and drawing 22.

[0005] The component isolation region 102 and the gate field 104 are formed in the base 100 which consists of a [process -10] semi-conductor substrate. Then, a LDD ion implantation is performed, the gate sidewall 106 is formed, an ion implantation is performed and the source drain field 108 is formed (refer to (A) of drawing 20).

[0006] The layer insulation layer 112 is formed all over after that [ [process -20] ], and, subsequently to the layer insulation layer 112, opening 114 is formed (refer to (B) of drawing 20).

[0007] After forming the adhesion layer 116 which consists of Ti/TiN/Ti all over [a process -30], next the layer insulation layer 112 which contains opening 114 in a spatter, the metal wiring layer 118 which consists of aluminum system alloy (for example, aluminum-1wt%Si) by the elevated-temperature aluminum spatter method is made to deposit on the whole surface. Then, the antireflection film 120 which consists of TiON is formed in the whole surface. And wiring is formed by carrying out patterning of an antireflection film 120, the metal wiring layer 118, and the adhesion layer 116 with a photolithography technique and a dry etching technique (refer to (C) of drawing 20).

[0008] [Process -40] Subsequently flattening processing by polish is performed. That is, the 1st insulator layer 122 which consists of SiO<sub>2</sub> by the plasma-CVD method all over the layer insulation layer 112 including wiring is formed, the stopper layer 124 which consists of SiN by the plasma-CVD method on it is formed, and the 2nd insulator layer 126 which consists of thick SiO<sub>2</sub> is further formed with a CVD method on it (refer to (A) of drawing 21).

[0009] The 2nd insulator layer 126 is ground from the upper part after that [ [process -50] ].

And it grinds until the stopper layer 124 appears as a polished surface (refer to (B) of drawing 21 ). In this way, the 1st insulator layer 122 by which flattening was carried out is formed after wiring.

[0010] Or the insulator layer by which flattening processing was carried out can also be formed at the following processes again instead of [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN.

[0011] The insulator layer 130 which consists of SiO<sub>2</sub> by the [process-40'] plasma-CVD method is formed.

[0012] After that [ [process-50'] ], a resist 132 is formed on an insulator layer 130, and patterning of the resist 132 is carried out so that the heights of an insulator layer 130 may be exposed (refer to (A) of drawing 22 ).

[0013] A resist 132 is removed after etching [process-60'], next the heights of an insulator layer 130 (refer to (B) of drawing 22 ).

[0014] a part of insulator layer 130 which remained after that [ [process-70'] ], without being etched -- 130A is ground and flattening of an insulator layer 130 is performed.

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## EFFECT OF THE INVENTION

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[Effect of the Invention] In this invention, the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring is unnecessary. Therefore, the scattered reflection of the light in the conventional photolithography technique, or the heterogeneity of etching and the problem of a corrosion in dry etching is avoidable.

[0159] Moreover, in production of a semiconductor device which has detailed wiring, flattening with a perfect insulating layer including wiring becomes possible, without performing formation of the insulator layer formed on wiring like before, or polish of this insulator layer. since the conventional SiO<sub>2</sub> system insulator layer was deficient in the selectivity in polish, the controllability of polish was scarce, but since the selectivity over an insulating layer is large, the controllability of polish is also boiled markedly and polish's of a metal wiring layer improves.

[0160] Furthermore, in order to leave a metal wiring layer only to a slot or opening circles, by adopting the etchback by the chemical mechanical polish method or the dry etching method, a Prior art can be used as it is fundamentally, and the manufacturing cost of a semiconductor device does not increase.

[0161] In addition, by forming a sidewall in a slot or opening circles, oxidation of a metal wiring layer can be prevented, moreover, by the metal wiring layer, it is stabilized and a slot or opening can be embedded.

[0162] In the wiring structure and the wiring formation approach concerning the 1st mode of this invention, since wiring structure is constituted from an Ag layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Furthermore, since resistance is lower than aluminum system alloy, Ag can expect the response speed of a semiconductor device.

[0163] In the wiring formation approach which starts the wiring structure concerning the 2nd mode of this invention, and a list at the 2nd and 3rd modes, since a metal wiring layer is constituted from a Cu layer which has electromigration-proof nature from aluminum system alloy, the dependability of a semiconductor device improves conventionally. Moreover, since the front face of Cu layer is covered with Ag layer, while preventing oxidation of Cu layer, wiring resistance can be kept low with the low resistance of Ag. Although Cu had the need for process limitation on problems, such as oxidation, conventionally, it becomes possible to use processes, such as heat treatment of an oxygen ambient atmosphere.

[0164] By the silver thin film formation approach of this invention, CVD of Ag becomes possible and the perfect embedding of Ag to a slot or opening becomes possible.

[0165] Furthermore, in the CVD system of this invention, since the source charging line to a CVD chamber and the connection of a CVD chamber can be held to high temperature, it is stabilized and material gas can be supplied.

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## TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] If wiring makes it detailed, it will become difficult to form the wiring width of face made into the purpose with a sufficient controllability. In response to the effect of the irregularity of the layer insulation layer 112 which is a substrate, irregularity arises in the front face of the metal wiring layer 118. Moreover, it is easy to be ruined when the metal wiring layer 118 which consists of aluminum system alloy is formed by the elevated-temperature aluminum spatter method etc. (that is, irregularity is easy to be formed). It originates in these and the coverage of the antireflection film 120 in the crevice of the metal wiring layer 118 falls (for example, refer to (C) of drawing 20 ). In order for the reflection factor of the light in the part to fall, the scattered reflection of light arises, and it becomes impossible consequently, to form the target patterning configuration to the metal wiring layer 118 under the effect of halation etc. as a result.

[0016] Moreover, the wiring structure after resist patterning is the 120/metal wiring layer 118 of antireflection films which consists of a top to TiON. Dry etching performs patterning of the metal wiring layer 118 after resist patterning. In this case, BCl<sub>3</sub> system gas is usually used as etching gas. However, etching by BCl<sub>3</sub> system gas is only a chemical reaction, and it is impossible to etch the antireflection film 120 which consists of TiON by BCl<sub>3</sub> system gas. So, it is necessary to etch the antireflection film 120 in a physical spatter operation.

[0017] Therefore, in case the metal wiring layer 118 which consists of aluminum system alloy is etched, it is necessary to change into chemical etching conditions from the etching conditions which have a spatter operation. However, when the thickness of the 120/metal wiring layer 118 of antireflection film is uneven, these etching serves as an ununiformity by modification of such etching conditions.

[0018] Furthermore, the approach explained at [the process -40] and [the process -50] using the stopper layer 124 which consists of SiN has the following troubles. That is, although the stopper layer 124 is used in case the 2nd insulator layer 126 which consists of SiO<sub>2</sub> is ground, the selection ratio to polish of SiO<sub>2</sub> and SiN is obtained three to about six. Therefore, it does not function as a stopper so that the stopper layer 124 which consists of SiN may perform the terminal point judging of polish, but the 1st insulator layer 122 may be ground too much. Namely, the 2nd insulator layer 126 cannot be ground with a sufficient controllability. Consequently, it has the problem that perfect flattening of the 1st insulator layer 122 cannot be attained.

[0019] And if spacing of wiring is thin in case between wiring is embedded by the 1st insulator layer 122 which consists of SiO<sub>2</sub> or SOG with a CVD method etc., the embedding of the 1st insulator layer 122 becomes inadequate, and it also has the problem that "\*\* (void)" 122A occurs in the 1st insulator layer 122 during wiring (refer to drawing 23 ).

[0020] on the other hand -- SiN -- from -- changing -- a stopper -- a layer -- 124 -- not using -- [-- a process - 40 -- ' --] -- [-- a process - 70 -- ' --] -- having explained -- an approach -- also setting -- an insulator layer -- 130 -- polish -- the time -- an insulator layer -- 130 -- polish -- a terminal point -- a judgment -- carrying out -- \*\*\*\* . For this reason, it has the problem of grinding an insulator layer 130 too much.

[0021] Thus, in manufacture of a detailed semiconductor device, after forming wiring, the conventional approach of forming a flat insulator layer on it has the above various troubles, and

there is still no approach for solving these troubles effectively.

[0022] In the above-mentioned process, aluminum system alloy is used as a wiring material. In the metal wiring layer 118 which consists of aluminum system alloy, electromigration is a big problem. Moreover, at the time of the dry etching of the metal wiring layer 118, by the corrosion of a metal wiring layer, a void occurs in a metal wiring layer and the dependability fall of wiring is caused. As a result of the aluminum particle in the metal wiring layer 118 moving when a current is passed to wiring as detailed wiring-ization progresses especially, current concentration arises in the minute chip void generated in the metal wiring layer. Therefore, it was missing with electromigration and much more dependability fall of wiring is caused by compound operation of a void.

[0023] Using copper (Cu) as a wiring material as a way stage which solves this problem is proposed. However, there is no suitable etching approach of Cu and it has various problems -- that the workability of Cu is not good, and heat treatment in the furnace which contains oxygen several% that it is very easy to oxidize cannot be performed. The problem of workability forms a slot in an insulating layer, and after making Cu deposit on an insulating layer including this slot, it can avoid it by grinding Cu on an insulating layer chemically and mechanically by the chemical mechanical polish method. However, an effective means to prevent oxidation of the front face of Cu embedded in the slot is not known.

[0024] Therefore, the 1st purpose of this invention does not need to perform the patterning process of the metal wiring layer by the photolithography technique and dry etching technique for forming wiring, and the insulating layer which includes wiring, without grinding the insulator. layer formed on wiring like before -- completeness -- it is in offering the wiring structure and the wiring formation approach of a new semiconductor device which make flattening possible and can solve the trouble at the time of using aluminum system alloy and Cu as a wiring material further.

[0025] The 2nd purpose of this invention is to offer the new silver thin film formation approach. Furthermore, the 3rd purpose of this invention is to provide the CVD system list suitable for application to this wiring structure and the wiring formation approach with the chemical mechanical polish method.

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MEANS

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[Means for Solving the Problem] the 1st voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom and Ag layer by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles -- since -- it is characterized by being constituted.

[0027] In the wiring structure of the semiconductor device concerning the 1st mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, in order to prevent oxidation of a metal wiring layer on the side attachment wall of a slot or opening, the sidewall which consists of SiN may be formed.

[0028] The wiring formation approach of the semiconductor device concerning the 1st mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (\*\*) -- the process which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0029] the 1st voice of this invention -- the wiring formation approach of the semiconductor device applied like -- setting -- formation of Ag layer -- Ag<sub>2</sub> -- it can carry out by the chemistry gaseous-phase depositing method using CO<sub>3</sub>, AgNO<sub>2</sub>, AgBr, or AgI as a raw material. Removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of a chemical mechanical polish process of a metal wiring layer, or an etchback process of a metal wiring layer. the chemical mechanical polish method -- setting -- the mixed water solution of I<sub>2</sub> and KI -- using -- the chemical mechanical polish of Ag layer -- it can carry out.

[0030] Moreover, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. The process which forms the sidewall which changes from SiN to the side attachment wall of a slot or opening after the process of (b) can be included further.

[0031] the 2nd voice of this invention for attaining the 1st above-mentioned purpose -- the multilayer metal wiring layer which consists of the adhesion layer from the bottom by which the wiring structure of the semiconductor device applied like was formed in the slot or opening formed in the insulating layer on a (b) base, a (b) slot, or opening circles, Cu layer, and Ag layer -- since -- it is characterized by being constituted.

[0032] In the wiring structure of the semiconductor device concerning the 2nd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, SiN or the sidewall which consists of Ag again may be formed in the side attachment wall of a slot or opening.

[0033] The wiring formation approach of the semiconductor device concerning the 2nd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, (\*\*) -- the process

which forms from the bottom the multilayer metal wiring layer which consists of an adhesion layer, Cu layer, and Ag layer on the insulating layer containing a slot or opening circles, and the process which removes the metal wiring layer on an insulating layer (Ha), and leaves a metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0034] In the wiring formation approach of the semiconductor device concerning the 2nd mode of this invention, removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of chemical mechanical polish processes of a metal wiring layer. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the metal wiring layer on the insulating layer in the process of (Ha) can consist of etchback processes of a metal wiring layer again.

[0035] The wiring formation approach of the semiconductor device concerning the 3rd mode of this invention for attaining the 1st above-mentioned purpose The process which forms a slot or opening in an insulating layer after forming an insulating layer on a (b) base, The process which forms from the bottom the 1st multilayer metal wiring layer which consists of an adhesion layer and Cu layer on the insulating layer containing a (b) slot or opening circles, The process which removes the 1st metal wiring layer on an insulating layer, and leaves the 1st metal wiring layer to a slot or opening circles, (Ha) the process which forms the 2nd metal wiring layer which consists of Ag layer on a (d) insulating layer and the 1st metal wiring layer, and the process which removes the 2nd metal wiring layer on a (e) insulating layer, and leaves the 2nd metal wiring layer to a slot or opening circles -- since -- it is characterized by changing.

[0036] the 3rd voice of this invention -- in the wiring formation approach of the semiconductor device applied like, removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of chemical mechanical polish processes. In this case, removal of Ag layer by the chemical mechanical polish is performed using the mixed water solution of I2 and KI. Or removal of the 1st metal wiring layer on the insulating layer in the process of (Ha) or removal of the 2nd metal wiring layer on the insulating layer in the process of (e) can consist of etchback processes again.

[0037] In the wiring formation approach of the semiconductor device concerning the 2nd or 3rd mode of this invention, an adhesion layer can consist of two-layer structure of the bottom to Ti layer, a TiN layer, and a Ti layer / TiN layer, or two-layer structure of the bottom to Ag layer / Ti layer. Moreover, the process which forms the sidewall which changes from SiN or Ag to the side attachment wall of a slot or opening after the process of (b) can be included further.

[0038] The formation approach of the silver thin film for attaining the 2nd above-mentioned purpose is characterized by depending  $\text{Ag}_2\text{CO}_3$  on the chemistry gaseous-phase depositing method used as a raw material. Or it is characterized by being based on the chemistry gaseous-phase depositing method using  $\text{AgNO}_2$  as a raw material again. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using  $\text{AgBr}$  as a raw material. Furthermore, it is characterized by being based on the chemistry gaseous-phase depositing method using  $\text{AgI}$  as a raw material. These raw materials are gasified and it uses as CVD gas using carrier gas, such as inert gas.

[0039] The CVD system of this invention for attaining the 3rd above-mentioned purpose is equipped with piping which connects the source of a raw material, a CVD chamber, and the source of a raw material and a CVD chamber. And it is characterized by having the 1st heater which heats piping more than the boiling point of a raw material, and the 2nd heater which heats the CVD chamber induction for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater can be used as lamp heating apparatus.

[0040] The chemical mechanical polish method for attaining the 3rd above-mentioned purpose is characterized by grinding a silver thin film chemically and mechanically using the mixed water solution of I2 and KI.

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## OPERATION

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[Function] The metal wiring layer is formed in a slot or opening circles in this invention. Such a metal wiring layer of a gestalt removes the metal wiring layer on an insulating layer, and since it is formed by leaving a metal wiring layer to a slot or opening circles, it does not need to perform patterning of the metal wiring layer formed on the insulating layer by the photolithography technique and the dry etching technique like the conventional technique. Moreover, since flattening processing by removal of the metal wiring layer on an insulating layer is performed, it is not necessary to perform flattening processing of the insulator layer formed on wiring like a Prior art.

[0042] Ag cannot oxidize easily due to elevated-temperature heat treatment. Although Ag also oxidizes, it decomposes into  $\text{AgO} \rightarrow \text{Ag} + \text{O}$  at the temperature more than 100-degreeC. For this reason, AgO is not stable at the temperature of hundreds of degreeC, and the oxide of Ag is not maintained. Moreover, since a metal wiring layer is constituted from Ag, the problem of electromigration like aluminum system alloy is not generated. Therefore, stable wiring can be formed in the wiring structure or the wiring formation approach concerning the 1st mode of this invention.

[0043] In the wiring formation approach concerning the wiring structure or the 2nd or 3rd mode concerning the 2nd mode of this invention, since a metal wiring layer is constituted from an Ag layer and a Cu layer, the problem of electromigration like aluminum system alloy is not generated. And since the front face of Cu layer is covered with Ag layer, oxidation of Cu layer can be prevented.

[0044] Hereafter, with reference to a drawing, this invention is explained based on an example. In addition, in an example 1 -- an example 6, the wiring formation approach concerning the wiring structure and the 1st mode of a semiconductor device concerning the 1st mode of this invention is explained. Moreover, in an example 7 -- an example 12, the wiring formation approach concerning the wiring structure and the 2nd mode of a semiconductor device concerning the 2nd mode of this invention is explained. Furthermore, in an example 13 -- an example 15, the wiring formation approach concerning the wiring structure and the 3rd mode of a semiconductor device concerning the 2nd mode of this invention is explained.

[0045] (Example 1) an example 1 -- an example 6 -- the 1st voice of this invention -- the wiring structure of the semiconductor device applied like, and the 1st voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 1 changes from the multilayer metal wiring layer 22 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 1 so that a sectional view may be shown in part. The metal wiring layer 22 consists of an adhesion layer 16 and an Ag layer 20 from the bottom. The adhesion layer 16 is the two-layer structure of Ti layer 18 A/TiN layer 18B from the bottom.

[0046] the wiring formation approach of an example 1 -- (\*\*) -- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10, and (\*\*) -- it consists of the process which forms from the bottom the multilayer metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and the process which remove the metal wiring layer 22 on an insulating layer (Ha) 12, and leave the metal wiring layer 22 in a slot 14 on

an insulating layer 12 including the inside of a slot 14. Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used  $\text{Ag}_2\text{CO}_3$  as a raw material. Moreover, removal of the metal wiring layer 22 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 22 of having used the mixed water solution of  $\text{I}_2$  and  $\text{KI}$ . By operating as a stopper the insulating layer 12 which consists of  $\text{SiO}_2$ , it becomes possible to set up the selection ratio of the metal wiring layer 22 and insulating layer 12 to a chemical mechanical polish to infinity.

[0047] Hereafter, with reference to typical drawing 2 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 1 is explained concretely.

[0048] The insulating layer 12 which consists of  $\text{SiO}_2$  is formed on the base 10 which consists of [a process -100, for example, a semi-conductor substrate.]. The formation conditions of an insulating layer 12 can be carried out as follows.

Gas used :  $\text{SiH}_4/\text{O}_2/\text{N}_2=250/250 / 100\text{sccm}$  substrate heating temperature: 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0049] A slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique after that [ [process -110] ] (refer to (A) of drawing 2 ). In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 2 . The conditions of dry etching can be carried out as follows.

Gas used :  $\text{C}_4\text{F}_8=50\text{sccm}$  RF power : 1200W pressure : 2Pa [0050] The adhesion layer 16 which consists of Ti layer 18 A/TiN layer 18B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -120] next (refer to (B) of drawing 2 ). The adhesion layer 16 can be formed on condition that the following.

Formation use gas 150 degreeC thickness of Ti layer 18A :  $\text{Ar}=100\text{sccm}$  power : 4kW pressure : 0.47Pa membrane formation temperature : : Formation use gas of 50nmTiN layer 18B :

$\text{Ar}/\text{N}_2=40/70\text{sccm}$  power : 5kW pressure : 0.47Pa thickness : 70nm [0051] The silver (Ag) layer 20 is formed in the whole surface with a CVD method after that [ [process -130] ] (refer to (C) of drawing 2 ). Formation of the Ag layer 20 is based on the chemistry gaseous-phase depositing method for having used  $\text{Ag}_2\text{CO}_3$  as a raw material. The conditions of CVD can be carried out as follows.

Raw material : Source temperature of  $\text{Ag}_2\text{CO}_3$  raw material : 170-degreeC use gas :  $\text{Ag}_2\text{CO}_3/\text{Ar}/\text{H}_2=10/25/1000\text{sccm}$  pressure :  $2.6 \times 10^3\text{Pa}$  substrate heating temperature: By this, the Ag layer 20 deposits on the 450-degreeC insulating layer 12 including the inside of a slot 14. The Ag layer 20 is formed of the following reaction.

$\text{Ag}_2\text{CO}_3 + \text{H}_2 \rightarrow 2\text{Ag} + \text{CO}_2 + \text{H}_2\text{O}$  [0052] The CVD system of this invention shown in drawing 3 for formation of the Ag layer 20 was used. This CVD system is equipped with the piping 204 which connects the CVD chamber 200, the source 202 of a raw material, the source of a raw material, and a CVD chamber. And it has the 1st heater 206 which heats piping 204 more than the boiling point of a raw material, and the 2nd heater 210 which heats the CVD chamber induction 208 for introducing a raw material into a CVD chamber more than the boiling point of a raw material. The 2nd heater 210 is lamp heating apparatus, and the mirror 212 is formed. Moreover, the aperture 214 made from a quartz is formed in the part of the about 208 CVD chamber induction [ which opposes the 2nd heater 210 ] piping 204. In addition, it is a heater for lamp heating apparatus for 216 to heat a base 10 and 218 to heat inert gas induction among drawing 3 , and for 220 heat the source 202 of a raw material. At the 1st and 2nd heaters 206, 210,  $\text{Ag}_2\text{CO}_3$  gas which flows the inside of piping 204 and the CVD chamber induction 208 is held more than 218-degreeC which is the boiling point.

[0053] By [a process -140], next the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 20 and the adhesion layer 16, and wiring which consists of the metal wiring layer 22 is formed (refer to drawing 1 ). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be carried out as follows.

Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force :  $5.5 \times 10^8\text{Pa}$  pad temperature : A chemical mechanical polish is performed using the mixed water solution of 40 degree  $\text{Cl}_2 + \text{KI}$ .

[0054] since a slurry (abrasive material +KOH+ water of SiO<sub>2</sub> system) is used when grinding SiO<sub>2</sub> conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO<sub>2</sub> is ground by the slurry -- grinding -- passing -- etc. -- the problem that dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 20 and the adhesion layer 16, a slurry is not needed, but by grinding with the mixed water solution of I<sub>2</sub>+KI, it is possible to remove only the Ag layer 20 and the adhesion layer 16, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.

[0055] Wiring which consists of the metal wiring layer 22 embedded at the flat insulating layer 12 by this is formed. In an example 1, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.

[0056] (Example 2) In the example 1, the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 22 is removed [ in / instead / an example 2 ] by the etchback method by dry etching. In addition, other processes are the same as an example 1, and detailed explanation is omitted.

[0057] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20 in a slot 14 for the Ag layer 20 and the adhesion layer 16 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 22] slot 14.

Gas used : NO<sub>2</sub>/O<sub>2</sub>=20 / 20sccm microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100-degreeC

[0058] (Example 3) In an example 3, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -110] of an example 1 and [a process -120] is included further. In addition, other processes are the same as an example 1, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 3 is explained with reference to drawing 5 . By forming a sidewall 26, oxidation of the adhesion layer 16 by the insulating layer 12 can be prevented.

[0059] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 5 ). The formation conditions of SiN layer 26A are illustrated below.

Gas used: SiH<sub>4</sub>/NH<sub>3</sub>/N<sub>2</sub>=180/500/720sccm temperature : 200-degreeC pressure : 40Pa

thickness : 100nm [0060] Then, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 5 ). The conditions of etchback can be carried out as follows.

Gas used : CHF<sub>3</sub>=50sccmRF power : 300W pressure : 2Pa of sidewalls 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 5 can be formed through [process -120] - [a process -140]. [ of an example.1 ]

[0061] (Example 4) The wiring structure of an example 4 typical to drawing 6 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 1 and a little and consists of a semi-conductor substrate, It consists of metal wiring layers 22 which consist of the adhesion layer 16 and the Ag layer 20 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 24 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 22.

[0062] The wiring formation approaches of an example 4 differ an example 1 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 22 which consists of the adhesion layer 16 and the Ag layer 20, and form wiring structure. The metal wiring layer 22 on

2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 4 is explained with reference to typical drawing 7 and typical drawing 8 which are sectional views a part, such as a semiconductor device.

[0063] On the base 10 which consists of the semi-conductor substrate which consists of [Process] -400 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, in order to form the gate sidewall 34 in the whole surface, SiO<sub>2</sub> film is made to deposit, after performing a LDD ion implantation. The deposition conditions of SiO<sub>2</sub> film can be carried out as follows.

Gas used : SiH<sub>4</sub>/O<sub>2</sub>-/N<sub>2</sub>=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : Further, whole surface etchback of SiO<sub>2</sub> film is performed and 0.25 micrometers of gate sidewalls 34 are formed in the side attachment wall of the gate field 32. Whole surface etchback can be performed on condition that the following.

Gas used : C<sub>4</sub>F<sub>8</sub>=50sccmRF power: 1200W pressure : An impurity ion implantation is performed on condition that the following after that [ 2Pa ] for formation of the source drain field 36. formation As of an N type channel Formation BF 2 of 20KeV and 5x10<sup>15</sup>-/cm<sup>2</sup> P type channel 20KeV and 3x10<sup>15</sup>-/cm<sup>2</sup> -- a part typical to (A) of drawing 7 in this way -- the structure shown with a sectional view can be acquired.

[0064] 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with the CVD method of the following conditions after that [ [process -410] ]. SiO two-layer formation use gas : TEOS 50sccm pressure : 40Pa temperature : 720-degreeC thickness : Formation use gas of 400nmBPSG layers : SiH<sub>4</sub>/PH<sub>3</sub>/B-2H<sub>6</sub>/O<sub>2</sub>/N<sub>2</sub>=80/7/7/1000/32000sccm temperature : 400-degreeC pressure : 1.0x10<sup>5</sup>Pa thickness : 500nm 900 more degreeC and reflow processing for 20 minutes are performed, and flattening of 1st insulating-layer 12A is performed.

[0065] [A process -420], next 2nd insulating-layer 12B which consists of SiO<sub>2</sub> are formed in the whole surface. 2nd insulating-layer 12B can be formed on condition that the following:

Gas used : SiH<sub>4</sub>/O<sub>2</sub>-/N<sub>2</sub>=250/250 / 100sccm temperature : 420-degreeC pressure : 13.3Pa thickness : 0.8 micrometers [0066] Slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -110] of an example 1 after that [ [process -430] ] (refer to (B) of drawing 7 ).

[0067] [Process -440] Subsequently opening 14A is formed in 1st insulating-layer 12A by performing dry etching after regist patterning (refer to (C) of drawing 7 ). Here, width of face of slot 14B is made larger than the path of opening 14A. The conditions of dry etching can be carried out as follows.

Gas used : C<sub>4</sub>F<sub>8</sub> 50sccmRF power: 1200W pressure : Further, 2Pa of 1100-degreeC and activation annealing for 10 seconds are performed, after forming a junction field by performing an ion implantation to opening circles. The following examples can be given as conditions for an ion implantation.

Formation As of an N type channel Formation BF 2 of 20KeV and 5x10<sup>15</sup>-/cm<sup>2</sup> P type channel 20KeV, 3x10<sup>15</sup>-/cm<sup>2</sup> [0068] It is desirable to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer subsequently like [the formation process of a sidewall 26] of an example 3, and to form the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the side attachment wall of slot 14B after that [ [process -450] ], (refer to (A) of drawing 8 ).

[0069] The adhesion layer 16 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -460] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.

[0070] The Ag layer 20 is formed in the whole surface like the [process -130] of an example 1 after that [ [process -470] ] by the chemistry gaseous-phase depositing method using Ag<sub>2</sub>CO<sub>3</sub> as a raw material (refer to (B) of drawing 8 ).

[0071] Like [a process -480], next the [process -140] of an example 1, by the chemical mechanical polish method, the Ag layer 20 and the adhesion layer 16 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 20 and the adhesion layer 16, and the connection hole and wiring which consist of

the metal wiring layer 22 are formed (refer to drawing 6 ). That is, the connection hole (for example, the so-called contact hole) with which the metal wiring layer 22 was embedded is formed in opening 14A. Moreover, the wiring 24 with which the metal wiring layer 22 was embedded at slot 14B is formed.

[0072] In addition, it is also removable by carrying out etchback by the dry etching method like an example 2 instead of removing the metal wiring layer 22 which consists of the Ag layer 20 and the adhesion layer 16 by the chemical mechanical polish method.

[0073] (Example 5) An example 5 is deformation of an example 4. Although the wiring structure of an example 5 is the same as an example 4, the wiring formation approach is different from an example 4. That is, opening 14A prepared in 1st insulating-layer 12A is embedded with the metal wiring material which consists of Ag, connection hole 24A is completed, subsequently to a it top, 2nd insulating-layer 12B is made to deposit, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 4. In an example 5, [the process -400], [a process -410], and [a process -440] of an example 4 are same process, and other processes differ. Hereafter, the approach of an example 5 is explained with reference to drawing 9 and drawing 10 .

[0074]

On the base 10 which consists of the semi-conductor substrate of [process -500] -[process -520] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for formation of the source drain field 36. Then, 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after resist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -400] of an example 4, [a process -410], and [a process -440]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.

[0075] [Process -530]

1st adhesion layer 16A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -520] by the same approach as the [process -120] of an example 1.

Subsequently, by the same approach as the [process -130] of an example 1, 1st Ag layer 20A is formed on the whole surface with a CVD method, and the 1st metal wiring layer which consists of 1st adhesion layer 16A and 1st Ag layer 20A is formed (refer to (A) of drawing 9 ).

[0076] After that [ [process -540] ], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 20A and 16A only in opening 14A (refer to (B) of drawing 9 ). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1. Of this, the so-called contact hole 24A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 20A and 16A only in opening 14A with the etchback by the dry etching method like an example 2.

[0077] [Process -550] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -420] of an example 4. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -430] of an example 4 (refer to (A) of drawing 10 ). Then, if needed, a SiN layer may be formed in the whole surface by the plasma-CVD method, subsequently whole surface etchback of the SiN layer may be carried out like the [process -450] of an example 4, and the sidewall (not shown) which changes from SiN to the side attachment wall of slot 14B by this may be formed.

[0078] By the same approach as [a process -560], next the [process -120] of an example 1 After forming in a spatter 2nd adhesion layer 16B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of

an example 1 2nd Ag layer 20B is formed on the whole surface with a CVD method, and the 2nd metal wiring layer which consists of 2nd adhesion layer 16B and 2nd Ag layer 20B is formed. [0079] [Process -570] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves 2nd Ag layer 20B and 2nd adhesion layer 16B, and wiring 24 is formed (refer to (B) of drawing 10 ). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -140] of an example 1.

[0080] In addition, instead of removing the 2nd metal wiring layer 20B and 16B on 2nd insulating-layer 12B by the chemical mechanical polish method, like an example 2, etchback of the 2nd metal wiring layer 20B and 16B is carried out by the dry etching method, it can leave the 2nd metal wiring layer 20B and 16B only in slot 14B, and wiring 24 can also be formed in slot 14B by this.

[0081] (Example 6) An example 6 is deformation of an example 5. The point that an example 6 is different from an example 5 is in the point which forms a tungsten plug with a CVD method in opening 14A beforehand. Hereafter, the wiring formation approach of an example 6 is explained with reference to drawing 11 .

[0082]

[Process -600] - [a process -620] These processes can be made to be the same as that of [process -500] - [a process -520]. [ of an example 5 ]

[0083] [Process -630]

The barrier layer 40 which consists of Ti/TiN is formed in the whole surface in a spatter after [a process -620], and the tungsten layer 42 is formed with a CVD method all over after that (refer to (A) of drawing 11 ). The membrane formation conditions of Ti and TiN can be made to be the same as that of the [process -120] of an example 1. Moreover, the membrane formation conditions of the tungsten by the CVD method are illustrated below.

Gas used : WF<sub>6</sub>/H<sub>2</sub>=95 / 550sccm membrane formation temperature : 450-degreeC pressure : 1.1x10<sup>4</sup>Pa thickness : 0.4 micrometers [0084] After that [ -[process -640] ], etchback is performed by the dry etching method, the tungsten layer 42 and the barrier layer 40 on 1st insulating-layer 12A are removed, and it leaves the metal plug and the barrier layer 40 which consist of the tungsten layer 42 only in opening 14A (refer to (B) of drawing 11 ). The conditions of dry etching can be carried out as follows.

Gas used : SF<sub>6</sub>=50sccm microwave power: 850WRF power : 150W pressure : Contact hole 24A which consists of the so-called tungsten plug by which the tungsten was embedded at opening 14A by this 1.33Pa is formed. In addition, it may leave the tungsten layer 42 and the barrier layer 40 only in opening 14A by the chemical mechanical polish method instead of the etchback by the dry etching method.

[0085] [Process -650] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -550] of an example 5. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -550] of an example 5. In addition, width of face of slot 14B is made larger than the path of opening 14A.

[0086] After forming in a spatter the adhesion layer 16 which consists of Ti of 30nm thickness by the same approach as [a process -660], next the [process -560] of an example 5 on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -130] of an example 1, the Ag layer 20 is formed on the whole surface with a CVD method, and the metal wiring layer which consists of the adhesion layer 16 and the Ag layer 20 is formed.

[0087] The metal wiring layer on 2nd insulating-layer 12B is removed with the etchback by the chemical mechanical polish method or dry etching after that [ [process -670] ] by the same approach as the [process -140] of an example 1. By this, it leaves a metal wiring layer only in slot 14B, and the wiring 24 which consisted of metal wiring layers which consist of the adhesion layer 16 and the Ag layer 20 in slot 14B is formed (refer to (C) of drawing 11 ).

[0088] (Example 7) an example 7 - an example 12 -- the 2nd voice of this invention -- the wiring structure of the semiconductor device applied like, and the 2nd voice -- it is related with the wiring formation approach which starts like. The wiring structure of an example 7 changes



from the multilayer metal wiring layer 50 formed in the slot 14 where a semiconductor device is typical, and which was formed in the insulating layer 12 on a base 10, and the slot 14 to drawing 12 so that a sectional view may be shown in part. The metal wiring layer 50 consists of an adhesion layer 52, a Cu layer 54, and an Ag layer 56 from the bottom. Moreover, the adhesion layer 52 is the two-layer structure of Ti layer 52 A/TiN layer 52B from the bottom.

[0089] the wiring formation approach of an example 7 -- (\*\*)-- the process which forms a slot 14 in an insulating layer 12 after forming an insulating layer 12 on a base 10; and (\*\*)-- it consists on an insulating layer 12 including a slot 14 of the process which forms from the bottom the multilayer metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and the process which removes the metal wiring layer 50 on an insulating layer (Ha) 12, and leaves a metal wiring layer in a slot 14.

[0090] Formation of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 is performed in a spatter. Moreover, removal of the metal wiring layer 50 on the insulating layer 12 in the process of (Ha) consists of the chemical mechanical polish process of the metal wiring layer 50. By operating as a stopper the insulating layer 12 which consists of SiO<sub>2</sub>, it becomes possible to set up the selection ratio of the metal wiring layer 50 and insulating layer 12 to a chemical mechanical polish to infinity.

[0091] Hereafter, with reference to typical drawing 13 which is sectional views a part, such as a semiconductor device, the wiring formation approach of an example 7 is explained concretely.

[0092] The insulating layer 12 which consists of SiO<sub>2</sub> is formed on the base 10 which consists of [a process -700, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 13. The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.

[0093] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a spatter on the insulating layer 12 including a slot 14 from under [a process -710] next (refer to (A) of drawing 13). The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.

[0094] The copper (Cu) layer 54 is formed in the whole surface in a spatter after that [ [process -720] ] (refer to (B) of drawing 13). The Cu layer 54 can be formed on the following spatter conditions.

Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 500nm [0095] The silver (Ag) layer 56 is formed in the whole surface in a spatter after that [ [process -730] ] (refer to (C) of drawing 13). The Ag layer 56 can be formed in the spatter of the following conditions.

Gas used : Ar=100sccm power : 10kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nm of front faces of the Cu layer 54 is covered with the Ag layer 56 in this way.

[0096] By [a process -740], next the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, in a slot 14, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and wiring which consists of the metal wiring layer 50 is formed (refer to drawing 12). The polish equipment shown in drawing 4 is used for a chemical mechanical polish.

The conditions of a chemical mechanical polish can be carried out as follows.

Polish plate rotational frequency : 37rpm substrate maintenance base rotational frequency : 17rpm polishing pressure force : 5.5x10<sup>8</sup>Pa pad temperature : The mixed water solution of I2+KI is used for removal by the chemical mechanical polish method of the 40-degreeCAg layer 56. Moreover, K<sub>4</sub>Fe(CN)<sub>6</sub>+H<sub>2</sub>O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.

[0097] since a slurry (abrasive material +KOH+ water of SiO<sub>2</sub> system) is used when grinding SiO<sub>2</sub> conventionally, but it is not distributed at homogeneity in the field which a slurry should grind in case SiO<sub>2</sub> is ground by the slurry -- grinding -- passing -- etc. -- the problem that

dispersion arises is in flattening of the polished surface in a substrate. When grinding the Ag layer 56, the Cu layer 54, and the adhesion layer 52, a slurry is not needed, but by grinding in the mixed water solution of  $I_2+KI$ , and  $K_4Fe(CN)_6$  water solution, it is possible to remove only the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and it has the advantage that there is also little dispersion, in flattening of the polished surface in a substrate.

[0098] Wiring which consists of the metal wiring layer 50 embedded at the flat insulating layer 12 by this is formed. In an example 7, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary.

[0099] (Example 8) In the example 7, the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on an insulating layer 12 was removed by the chemical mechanical polish method. The metal wiring layer 50 is removed [ in / instead / an example 2 ] by the etchback method by dry etching. In addition, other processes are the same as an example 7, and detailed explanation is omitted.

[0100] Etchback is carried out by the dry etching method of the following conditions, and it leaves the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 in a slot 14 for the Ag layer 56, the Cu layer 54, and the adhesion layer 52 which were formed on the insulating layer 12 including the [etching process of metal wiring layer 50] slot 14. The etching use gas of the Ag layer 56 :  $NO_2/O_2=20 / 20sccm$  microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : Etching use gas of the 100-degreeCCu layer 54 and the adhesion layer 52 :  $O_2-Cl_2=10 / 70sccm$  microwave power: 1000WRF power : 300W pressure : 0.5Pa substrate heating temperature : 300-degreeC [0101]

(Example 9) In an example 9, the process which forms the sidewall 26 which changes from SiN to the side attachment wall of a slot 14 between the [process -710] of an example 7 and [a process -720] is included further. In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall 26 of an example 9 is explained with reference to drawing 14. By forming a sidewall 26, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.

[0102] SiN layer 26A is made to deposit by the plasma-CVD method the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall 26] slot 14 (refer to (A) of drawing 14). Next, whole surface etchback of the SiN layer 26A is carried out (refer to (B) of drawing 14). The formation conditions of SiN layer 26A and the conditions of etchback can be made to be the same as that of an example 3. A sidewall 26 is formed in the side attachment wall of a slot 14 of this. Henceforth, the wiring structure shown in (C) of drawing 14 can be formed through [process -720] - [a process -740]. [ of an example 7 ]

[0103] (Example 10) The sidewall 26 which consists of SiN in an example 9 was formed in the side attachment wall of a slot 14. On the other hand, in an example 10, a sidewall is formed from Ag (silver). In addition, other processes are the same as an example 7, and detailed explanation is omitted. Hereafter, the formation process of the sidewall of an example 10 is explained. By forming the sidewall which consists of Ag, oxidation of the adhesion layer 52 by the insulating layer 12 and the Cu layer 54 can be prevented.

[0104] Ag layer is made to deposit in a spatter the whole surface on the insulating layer 12 including the inside of the [formation process of sidewall which consists of Ag] slot 14. Next, whole surface etchback of the Ag layer is carried out. The formation conditions of Ag layer and the conditions of etchback are illustrated below.

Ag stratification condition use gas : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 100nmAg layer etchback condition use gas :  $NO_2/O_2=20 / 20sccm$  microwave power: 850WRF power : 10W pressure : 1.3Pa substrate heating temperature : 100degreeC -- the same sidewall can be formed in the side attachment wall of a slot 14 with having been shown in drawing 14 in this way. Henceforth, the same wiring structure can be formed with having been shown in (C) of drawing 14 through [process -720] - [a process -740]. [ of an example 7 ]



[0105] (Example 11) The wiring structure of an example 11 typical to drawing 15 which shows a sectional view in part Opening 14A formed in 1st insulating-layer 12A on the base 10 which differ an example 7 and a little and consists of a semi-conductor substrate. It consists of metal wiring layers 50 which consist of the adhesion layer 52, the Cu layer 54, and the Ag layer 56 which were embedded at slot 14B formed in 2nd insulating-layer 12B formed on 1st insulating-layer 12A, and opening 14A and slot 14B. In this case, the sidewall 26 which changes from SiN to the side attachment wall of opening 14A and the flank of slot 14B may be formed. Moreover, a lower layer conductor layer (for example, source drain field 36) and the wiring 58 in slot 14B are electrically connected by embedding opening 14A by the metal wiring layer 50.

[0106] The wiring formation approaches of an example 11 differ an example 7 and a little, after they form slot 14B in 2nd insulating-layer 12B formed on 1st insulating-layer 12A in opening 14A again at 1st insulating-layer 12A on the base 10 which consists of a semi-conductor substrate beforehand, embed opening 14A and slot 14B by the metal wiring layer 50 which consists of the adhesion layer 52, the Cu layer 54, and the Ag layer 56, and form wiring structure. The metal wiring layer 50 on 2nd insulating-layer 12B is removed by the chemical mechanical polish method. Hereafter, the wiring formation approach of an example 11 is explained with reference to typical drawing 16 which is sectional views a part, such as a semiconductor device.

[0107] On the base 10 which consists of the semi-conductor substrate of [Process] -1100 Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation.

[0108] After that [ [process -1110] ], 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed.

[0109] [Process -1120] Subsequently to a 1st insulating-layer 12A top, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed.

[0110] Slot 14B is formed in 2nd insulating-layer 12B after that [ [process -1130] ].

[0111] [Process -1140] Opening 14A is further formed in 1st insulating-layer 12A. Subsequently, activation annealing is performed after making a junction field form by performing an ion implantation to opening circles.

[0112] The above process can be made to be the same as that of [process -400] - [a process -440]. [ of an example 4 ]

[0113] [Process -1150] Subsequently the sidewall 26 which consists of SiN may be formed in the side attachment wall of opening 14A and slot 14B like the [process -450] of an example 4. Of the above process, the structure shown in (A) of drawing 16 is formed.

[0114] The adhesion layer 52 which consists of Ti layer / TiN layer is formed in a spatter from under [a process -1160] next on 2nd insulating-layer 12B containing opening 14A and slot 14B. This process can be made to be the same as that of the [process -120] of an example 1.

[0115] The Cu layer 54 is formed in the whole surface in a spatter like the [process -720] of an example 7 after that [ [process -1170] ]. Subsequently, the Ag layer 56 is formed in the whole surface in a spatter like the [process -730] of an example 7 (refer to (B) of drawing 16 ).

[0116] After that [ [process -1180] ], like the [process -740] of an example 7, by the chemical mechanical polish method, the Ag layer 56, the Cu layer 54, and the adhesion layer 52 on 2nd insulating-layer 12B are ground chemically and mechanically, and are removed, in slot 14B and opening 14A, it leaves the Ag layer 56, the Cu layer 54, and the adhesion layer 52, and the connection hole and wiring which consist of the metal wiring layer 50 are formed (refer to drawing 15 ). That is, connection hole 58A (for example, the so-called contact hole) where the metal wiring layer 50 was embedded is formed in opening 14A. Moreover, the wiring 58 with which the metal wiring layer 50 was embedded at slot 14B is formed.

[0117] In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the metal wiring layer 50 which consists of the Ag layer 56, the Cu layer 54, and the adhesion layer 52 by the chemical mechanical polish method.

[0118] (Example 12) An example 12 is deformation of an example 11. Although the wiring structure of an example 12 is the same as an example 11, the wiring formation approach is

different from an example 11. That is, after embedding opening 14A prepared in 1st insulating-layer 12A with the metal wiring material which consists of Cu and completing connection hole 58A, 2nd insulating-layer 12B is made to deposit on it, and the point which forms slot 14B in this 2nd insulating-layer 12B is different from an example 11. In an example 12, [the process -1100], [a process -1110], and [a process -1140] of an example 11 are same process, and other processes differ. Hereafter, the approach of an example 12 is explained with reference to drawing 17.

[0119]

On the base 10 which consists of the semi-conductor substrate of [process -1200] -[process -1220] Si (100), the component isolation region 30 and the gate field 32 are formed by the usual approach. Subsequently, after performing a LDD ion implantation, the gate sidewall 34 is formed and an impurity ion implantation is performed for source drain field formation. Then, 1st insulating-layer 12A which consists of two-layer [ of SiO<sub>2</sub> and BPSG ] is formed in the whole surface with a CVD method, reflow processing is performed, and flattening of 1st insulating-layer 12A is performed. Subsequently, activation annealing is performed after making a junction field form by forming opening 14A in 1st insulating-layer 12A in the dry etching after resist patterning, and performing an ion implantation to it at opening circles. These processes can be made to be the same as that of the [process -1100] of an example 4, [a process -1110], and [a process -1140]. Subsequently, the sidewall (not shown) which consists of SiN may be formed in the side attachment wall of opening 14A.

[0120] [Process -1230]

1st adhesion layer 52A which consists of Ti/TiN is formed in the whole surface from the bottom after [a process -1220] by the same approach as the [process -710] of an example 7.

Subsequently, by the same approach as the [process -720] of an example 7, 1st Cu layer 54A is formed on the whole surface in a spatter, and the 1st metal wiring layer which consists of 1st adhesion layer 52A and 1st Cu layer 54A is formed.

[0121] After that [ [process -1240] ], the 1st metal wiring layer on 1st insulating-layer 12A is removed by the chemical mechanical polish method, and it leaves the 1st metal wiring layer 54A and 52A only in opening 14A (refer to (A) of drawing 17 ). The conditions of a chemical mechanical polish can be made to be the same as that of the chemical mechanical polish of Cu layer of the [process -740] of an example 7. Of this, the so-called contact hole 58A by which the 1st metal wiring layer was embedded at opening 14A is formed. Instead of the chemical mechanical polish method, it may leave the 1st metal wiring layer 54A and 52A only in opening 14A with the etchback by the dry etching method like an example 8.

[0122] [Process -1250] Subsequently to the whole surface, 2nd insulating-layer 12B which consists of SiO<sub>2</sub> is formed. 2nd insulating-layer 12B can be formed on the same conditions as the [process -1120] of an example 11. Then, slot 14B is formed in 2nd insulating-layer 12B with a photolithography technique and a dry etching technique like the [process -1130] of an example 11. Then, subsequently it can form and be easy to form a SiN layer in the whole surface by the plasma-CVD method, to carry out whole surface etchback of the SiN layer, and to have the sidewall (not shown) which consists of SiN in the side attachment wall of slot 14B by this if needed, like the [process -1150] of an example 11.

[0123] By the same approach as [a process -1260], next the [process -710] of an example 7 After forming in a spatter 2nd adhesion layer 52B which consists of Ti with a thickness of 30nm on 2nd insulating-layer 12B containing slot 14B, by the same approach as the [process -730] of an example 7 The 2nd metal wiring layer which consists of 2nd adhesion layer 52B, 2nd Cu layer 54B, and the Ag layer 56 is formed by forming 2nd Cu layer 54B on the whole surface in a spatter, and forming the Ag layer 56 in a spatter on it further.

[0124] [Process -1270] Subsequently, by the chemical mechanical polish method, the 2nd metal wiring layer 56, 54B, and 52B on 2nd insulating-layer 12B is removed, in slot 14B, it leaves the Ag layer 56, Cu layer of \*\* 2nd 54B, and 2nd adhesion layer 52B, and wiring 58 is formed (refer to (B) of drawing 18 ). The conditions of a chemical mechanical polish can be made to be the same as that of the [process -740] of an example 7.

[0125] In addition, instead of removing the 2nd metal wiring layer 56, 54B, and 52B on 2nd

insulating-layer 12B by the chemical mechanical polish method. Like an example 8, etchback of the 2nd metal wiring layer 56, 54B, and 52B is carried out by the dry etching method, by this, it can leave the 2nd metal wiring layer 56, 54B, and 52B only in slot 14B, and wiring 58 can also be formed in slot 14B.

[0126] (Example 13) an example 7 - an example 12 -- setting -- the wiring structure of a semiconductor device -- the 2nd voice of this invention -- it formed by the wiring formation approach which starts like. On the other hand, the wiring structure of the semiconductor device in an example 13 - an example 15 is formed by the wiring formation approach concerning the 3rd mode of this invention.

[0127] The process which forms a slot 14 in an insulating layer 12 after the wiring formation approach of the semiconductor device of an example 13 forms an insulating layer 12 on the (b) base 10. The process which forms from the bottom 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 on the insulating layer 12 including the (b) slot 14. The process which removes 1st metal wiring layer 50A on an insulating layer 12, and leaves 1st metal wiring layer 50A in a slot 14, (Ha) It consists of the process which forms 2nd metal wiring layer 50B which consists of Ag layer on the (d) insulating layer 12 and 1st metal wiring layer 50A, and the process which removes 2nd metal wiring layer 50B on the (e) insulating layer 12, and leaves 2nd metal wiring layer 50B in a slot 14.

[0128] The adhesion layer 52, the Cu layer 54, and formation at metal wiring layer 50B to the 2nd are performed in a sputter. Moreover, removal of 2nd metal wiring layer 50B on the insulating layer 12 in the process of (e) changes from the chemical mechanical polish process of the metal wiring layer 50 to removal of 1st metal wiring layer 50A on the insulating layer 12 in the process of (Ha), and a list. By operating as a stopper the insulating layer 12 which consists of SiO<sub>2</sub>, it becomes possible to set up the selection ratio of the 1st [ to a chemical mechanical polish ], and 2nd metal wiring layers 50A and 50B, and an insulating layer 12 to infinity.

[0129] In the wiring formation approach concerning the 3rd mode of this invention, the Cu layer 54 can be covered with 2nd metal wiring layer 50B which consists of Ag layer much more more certainly than the wiring formation approach concerning the 2nd mode of this invention.

[0130] Hereafter, with reference to typical drawing 18 and typical drawing 19 which are sectional views a part, such as a semiconductor device, the wiring formation approach of an example 13 is explained concretely.

[0131] The insulating layer 12 which consists of SiO<sub>2</sub> is formed on the base 10 which consists of [a process -1300, for example, a semi-conductor substrate,]. The formation conditions of an insulating layer 12 can be made to be the same as that of the [process -100] of an example 1. Then, a slot 14 is formed in an insulating layer 12 with a photolithography technique and a dry etching technique. In addition, the slot 14 has extended in the direction perpendicular to the space of drawing 18. The conditions of dry etching can be made to be the same as that of the [process -110] of an example 1.

[0132] The adhesion layer 52 which consists of Ti layer 52 A/TiN layer 52B is formed in a sputter on the insulating layer 12 including a slot 14 from under [a process -1310] next. The adhesion layer 52 can be made to be the same as that of the [process -120] of an example 1.

[0133] The copper (Cu) layer 54 is formed in the whole surface in a sputter after that [ [process -1320] ] (refer to (A) of drawing 18 ). Formation of the Cu layer 54 can be made to be the same as that of the [process -720] of an example 7. In this way, 1st multilayer metal wiring layer 50A which consists of the adhesion layer 52 and the Cu layer 54 can be formed from the bottom on the insulating layer 12 including a slot 14.

[0134] By [a process -1330], next the chemical mechanical polish method, the Cu layer 54 and the adhesion layer 52 on an insulating layer 12 are ground chemically and mechanically, and are removed, and it leaves 1st metal wiring layer 50A which consists of the Cu layer 54 and the adhesion layer 52 in a slot 14 (refer to (B) of drawing 18 ). The polish equipment shown in drawing 4 is used for a chemical mechanical polish. The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. K<sub>4</sub>Fe(CN)<sub>6</sub>+H<sub>2</sub>O is used for removal by the chemical mechanical polish method of the Cu layer 54 and the adhesion layer 52.

[0135] 2nd metal wiring layer 50B which consists of a silver (Ag) layer is formed in the whole

surface in a spatter after that [ [process -1340] ] (refer to (A) of drawing 19 ). Formation of Ag layer can be made to be the same as that of the [process -730] of an example 13. In this way, the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B which consists of Ag layer.

[0136] By [a process -1350], next the chemical mechanical polish method, 2nd metal wiring layer 50B which consists of Ag layer on an insulating layer 12 is ground chemically and mechanically, and is removed, it leaves 2nd metal wiring layer 50B which consists of Ag layer in a slot 14, and wiring which consists of the 1st and 2nd metal wiring layers 50A and 50B is formed (refer to (B) of drawing 19 ). The conditions of a chemical mechanical polish can be made to be the same as that of an example 13. In addition, the mixed water solution of I<sub>2</sub>+KI is used for removal by the chemical mechanical polish method of Ag layer.

[0137] In an example 13, like the conventional wiring formation approach, resist-patterning processing and dry etching processing of a metal wiring layer become unnecessary, and the problem of dispersion of the light at the time of resist patterning and the problem from which etching becomes uneven can be avoided. Moreover, formation of the insulator layer on wiring and flattening processing of this insulator layer are also unnecessary. Moreover, since the front face of 1st metal wiring layer 50A is covered with 2nd metal wiring layer 50B much more certainly, oxidation of the Cu layer 54 which constitutes 1st metal wiring layer 50A can be prevented.

[0138] In an example 13, although 1st metal wiring layer 50A and 2nd metal wiring layer 50B were chiefly removed by the chemical mechanical polish method, it is also removable like an example 8 with the etchback by the dry etching method.

[0139] Moreover, formation of the sidewall explained in the wiring formation approach, and the example 9 or example 10 of the semiconductor device concerning the 3rd mode of this invention explained in the example 13 is also combinable. Furthermore, the wiring formation approach explained in the example 13 is also applicable instead of the Ag layer 56 in an example 11 or an example 12.

[0140] (Example 14) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 11 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0141] Formation of the component isolation region to a [process -1400] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.

[Process -1410] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [ of SiO<sub>2</sub> and BPSG ].

[Process -1420] Formation of the 2nd insulating layer which consists of SiO<sub>2</sub> to a 1st insulating-layer top.

Formation of the slot to the 2nd insulating layer of [a process -1430].

Formation of opening to the 1st insulating layer of [a process -1440].

Formation by the spatter to a 2nd insulating-layer top including opening and the slot of an adhesion layer which consist of a [process -1450] Ti layer / TiN layer.

Formation of Cu layer by the spatter to a [process -1460] adhesion layer top.

Removal of Cu layer on the 2nd insulating layer by the [process -1470] chemical mechanical polish.

Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1470] surface.

Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1480] chemical mechanical polish method.

[0142] (Example 15) Only the flow of the process in the case of applying the wiring formation approach explained in the example 13 instead of the Ag layer 56 in an example 12 is explained below. In addition, it is also removable by carrying out etchback by the dry etching method like an example 8 instead of removing the 1st and/or 2nd metal wiring layer by the chemical mechanical polish method.

[0143] Formation of the component isolation region to a [process -1500] base top, and a gate field. LDD ion implantation. Formation of a gate sidewall. The impurity ion implantation for source drain field formation.

[Process -1510] Formation and reflow processing of the 1st of an insulating layer which consist of two-layer [ of SiO<sub>2</sub> and BPSG ].

Formation of opening to the 1st insulating layer of [a process -1520].

[Process -1530] Formation by the spatter of the 1st metal wiring layer which consists of the 1st adhesion layer to a 1st insulating-layer top, and 1st Cu layer.

Removal of the 1st metal wiring layer on the 1st insulating layer by the [process -1540] chemical mechanical polish method. By this, the so-called contact hole where the 1st metal wiring layer was embedded at opening is formed.

Formation of the 2nd insulating layer which consists of SiO<sub>2</sub> all over [a process -1550].

Formation of the slot to the 2nd insulating layer.

[Process -1560] Formation by the spatter of the 2nd adhesion layer to a 2nd insulating-layer top, and Cu layer.

Removal of Cu layer on the 2nd insulating layer by the [process -1570] chemical mechanical polish, and the 2nd adhesion layer.

Formation of the 2nd metal wiring layer which changes from Ag layer by the spatter to the whole [process -1580] surface.

Removal of the 2nd metal wiring layer on the 2nd insulating layer by the [process -1590] chemical mechanical polish method.

[0144] As mentioned above, although this invention was explained based on the desirable example, this invention is not limited to these examples. The various ingredients and the conditions of having used in the example are instantiation, and can be changed suitably. Depending on the case, opening can be formed instead of Slots 14 and 14B.

[0145] Although the insulating layer was explained as what consists of the combination of SiO<sub>2</sub> or SiO<sub>2</sub>, and BPSG chiefly, it can constitute from what carried out the laminating of well-known insulating materials, such as BPSG, PSG and BSG, AsSG, PbSG, SbSG, SOG, SiON, or SiN, or these insulating layers to instead of [ these ].

[0146] In an example 1 - an example 6, although formation of the Ag layer 20 was performed by the chemistry gaseous-phase depositing method for having used Ag<sub>2</sub>CO<sub>3</sub> as a raw material instead, it can be performed by the chemistry gaseous-phase depositing method using AgNO<sub>2</sub>, AgBr, or AgI as a raw material. The CVD conditions in these cases and the heating conditions of the material gas which flows the inside of piping 204 and the CVD chamber induction 208 at the 1st and 2nd heaters 206,210 in the CVD system shown in drawing 3 are illustrated and combined with below, and a reaction formula is shown.

[0147] raw material: -- source temperature of AgNO<sub>2</sub> raw material 450-degreeC gas heating condition: -- more than 140-degreeC -- reaction-formula : 2AgNO<sub>2</sub>+7H<sub>2</sub>-

>2Ag+2NH<sub>3</sub>\*\*+4H<sub>2</sub>O\*\* : 150-degreeC use gas : AgNO<sub>2</sub>/Ar/H<sub>2</sub>=10/25/1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature : [0148] Raw material: Source temperature of an AgBr raw material : 450-degreeC use gas : AgBr/Ar/H<sub>2</sub>=10/75 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature: 500-degreeC gas heating conditions: It is power more than 434-degreeC. : 500W (plasma CVD)

Reaction formula : 2AgBr+H<sub>2</sub>->2Ag+2HBr\*\* [0149] Raw material: Source temperature of an AgI raw material : 560-degreeC use gas : AgI/Ar/H<sub>2</sub>=10/100 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature: 600-degreeC gas heating conditions: It is power more than 552-degreeC. : 500W (plasma CVD)

Reaction formula : 2AgI+H<sub>2</sub>->2Ag+2HI\*\* [0150] In an example 7 - an example 15, it can form with a CVD method instead of forming Cu layer and/or Ag layer in a spatter. The formation conditions of Cu layer by the CVD method are illustrated below.

Gas used : Cu (HFA)2/H<sub>2</sub>=10 / 1000sccm pressure : 2.6x10<sup>3</sup>Pa substrate heating temperature: 350-degreeC power : It is the abbreviation for hexafluoro acetylacetonate in 500W, in addition HFA.

[0151] An adhesion layer can also consist of a Ti layer or a TiN layer instead of Ti layer / TiN

layer. The formation conditions of the Ti layer or the TiN layer in this case can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1, and TiN layer 18B. Or an adhesion layer can also be made into the two-layer structure of Ag layer / Ti layer from the bottom again. In this case, Ag layer can be formed in the sputter of the following conditions. Moreover, the formation conditions of Ti layer can be made to be the same as that of the formation conditions of Ti layer 18A explained at the [process -120] of an example 1.

Sputter condition use gas of Ag layer : Ar=100sccm power : 4kW pressure : 0.47Pa membrane formation temperature : 200-degreeC thickness : 50nm [0152] TiON and TiW can also be used instead of TiN which constitutes an adhesion layer. Moreover, by the case, the sequence of formation of a slot, formation of a sidewall, and formation of an adhesion layer can be changed, and it can also consider as the order of formation of a slot, formation of an adhesion layer, and formation of a sidewall. Moreover, the metal layer or metallic-compounds layer which constitutes adhesion layers, such as Ti and TiN, can be formed by the forming-membranes methods, such as CVD.

[0153] The silicon layer formed on the various substrates for producing the various component sections, such as an insulating layer in which the MgO substrate, the GaAs substrate, superconducting transistor substrate, and lower layer wiring layer other than a silicon semiconductor substrate or the semi-conductor substrate with which the source drain field was formed were formed as a base, and a gate electrode which needs to form a connection hole ( a contact hole, a beer hall, through hole), and needs to form electrical installation, and a thin film transistor can be mentioned.

[0154] In an example 6, although the tungsten plug was formed in opening 14A using the so-called blanket tungsten CVD method, a tungsten plug may be instead formed in opening 14A with the so-called tungsten selection CVD method. The conditions in this case can be carried out as follows. Gas used : WF6/SiH4/H2/Ar=10/7/1000/10 sccm \*\* Whenever : 260-degreeC \*\* Force : 26Pa [0155] This invention is applicable to other semiconductor devices other than an MOS semiconductor device (for example, a bipolar transistor, CCD).

[0156] Various kinds of sputtering systems, such as a magnetron sputtering system, DC sputtering system, RF sputtering system, an ECR sputtering system, and a bias sputtering system that impresses substrate bias, can perform a sputter.

[0157] In the wiring structure concerning the 1st mode of this invention under Ag layer again the 2nd voice of this invention -- the wiring structure which starts like -- setting -- the bottom of Cu layer -- or -- again -- the wiring layer or connection hole under an adhesion layer -- refractory metals, such as Mo and Ti, -- Or a monolayer or various combination \*\*\*\*\* can be formed for the silicide of TiW, ZrN, W, WC, TiC, other MoSi2 and WSi2, and TiSi2 grade etc.

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[Translation done.]

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is typical drawing of the wiring structure of the semiconductor device of an example 1.

[Drawing 2] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 1 ] -- it is a sectional view a part.

[Drawing 3] It is the mimetic diagram of the CVD system of this invention.

[Drawing 4] It is the mimetic diagram of the polish equipment suitable for operation of this invention.

[Drawing 5] typical [ semiconductor device / for explaining the sidewall formation process of an example 3 ] -- it is a sectional view a part.

[Drawing 6] It is typical drawing of the wiring structure of the semiconductor device of an example 4.

[Drawing 7] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 4 ] -- it is a sectional view a part.

[Drawing 8] typical [ semiconductor device / for continuing at drawing 7 and explaining each process of the wiring formation approach of an example 4 ] -- it is a sectional view a part.

[Drawing 9] typical [ semiconductor device / for explaining the process of the wiring formation approach of an example 5 ] -- it is a sectional view a part.

[Drawing 10] typical [ semiconductor device / for continuing at drawing 9 and explaining the process of the wiring formation approach of an example 5 ] -- it is a sectional view a part.

[Drawing 11] typical [ semiconductor device / for explaining the process of the wiring formation approach of an example 6 ] -- it is a sectional view a part.

[Drawing 12] It is typical drawing of the wiring structure of the semiconductor device of an example 7.

[Drawing 13] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 7 ] -- it is a sectional view a part.

[Drawing 14] typical [ semiconductor device / for explaining the sidewall formation process of an example 9 ] -- it is a sectional view a part.

[Drawing 15] It is typical drawing of the wiring structure of the semiconductor device of an example 11.

[Drawing 16] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 11 ] -- it is a sectional view a part.

[Drawing 17] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 12 ] -- it is a sectional view a part.

[Drawing 18] typical [ semiconductor device / for explaining each process of the wiring formation approach of an example 13 ] -- it is a sectional view a part.

[Drawing 19] typical [ semiconductor device / for continuing at drawing 18 and explaining each process of the wiring formation approach of an example 13 ] -- it is a sectional view a part.

[Drawing 20] typical [ semiconductor device / for explaining each process in the example of a manufacture process of the conventional semiconductor device ] -- it is a sectional view a part.

[Drawing 21] typical [ semiconductor device / for explaining each process in the example of a

manufacture process of the conventional semiconductor device following on drawing 20 ] -- it is a sectional view a part.

[Drawing 22] typical [ semiconductor device / for explaining each process in another example of the manufacture process of the conventional semiconductor device ] -- it is a sectional view a part.

[Drawing 23] It is drawing for explaining the trouble in the manufacture process of the conventional semiconductor device.

[Description of Notations]

10 Base

12, 12A, 12B Insulating layer

14 14B Slot

14A Opening

16, 16A, 16B Adhesion layer

18A Ti layer

18B TiN layer

20 Ag Layer

22 Metal Wiring Layer

24 Wiring

24A Connection hole

26A SiN layer

26 Sidewall

30 Component Isolation Region

32 Gate Field

34 Gate Sidewall

36 Source Drain Field

40 Barrier Layer

42 Tungsten Layer

50 Metal Wiring Layer

50A The 1st metal wiring layer

50B The 2nd metal wiring layer

52, 52A, 52B Adhesion layer

54, 54A, 54B Cu layer

56 Ag Layer

58 Wiring

58A Connection hole

200 CVD Chamber

202 Source of Raw Material

204 Piping

206 1st Heater

208 CVD Chamber Induction

210 2nd Heater

214 Aperture

216 Lamp Heating Apparatus

218 Inert Gas Induction

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[Translation done.]



\* NOTICES \*

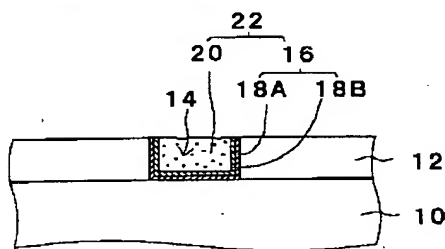
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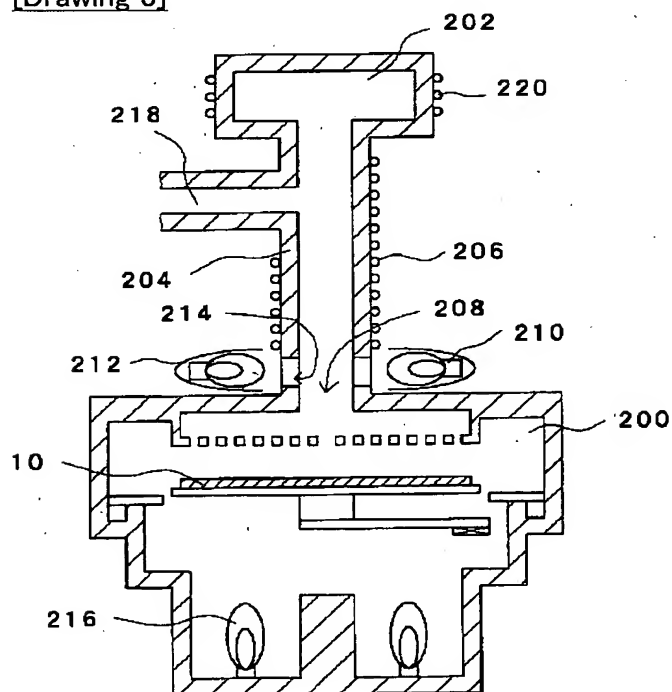
DRAWINGS

[Drawing 1]

(実施例1の配線構造)

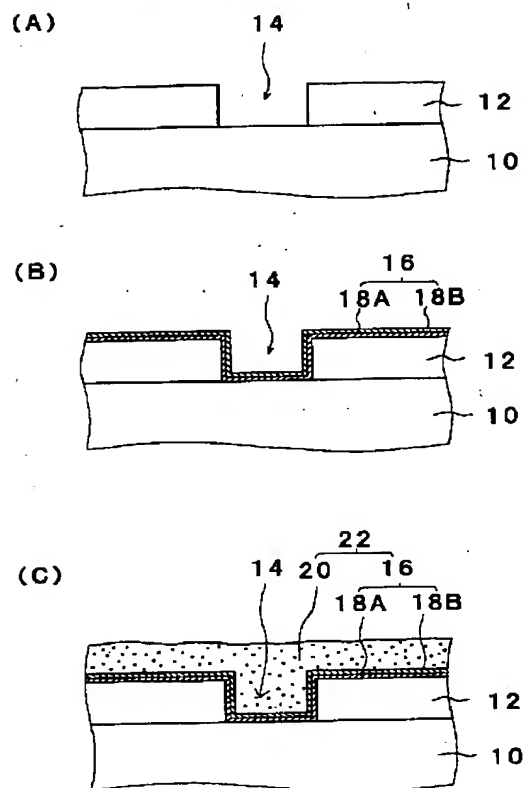


[Drawing 3]

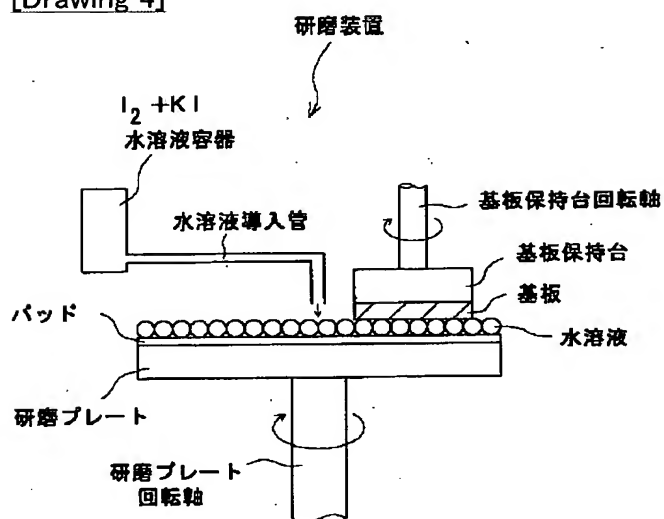


[Drawing 2]

## (実施例1の配線形成方法)



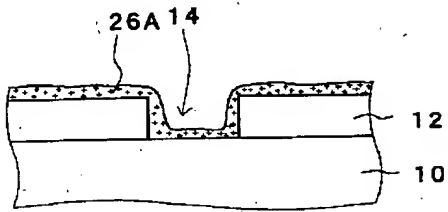
[Drawing 4]



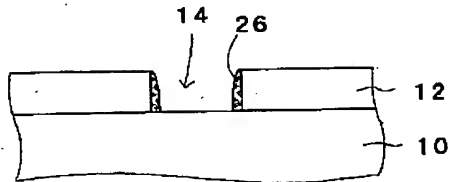
[Drawing 5]

(実施例3の配線形成方法)

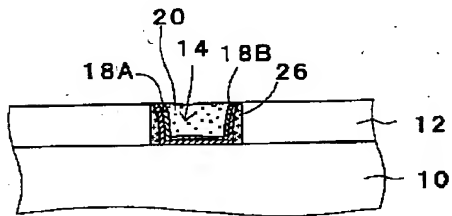
(A)



(B)

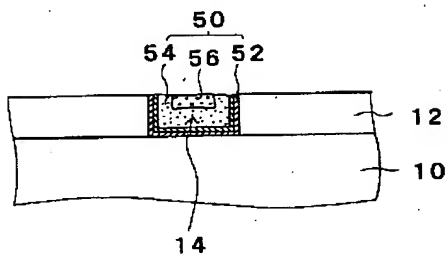


(C)



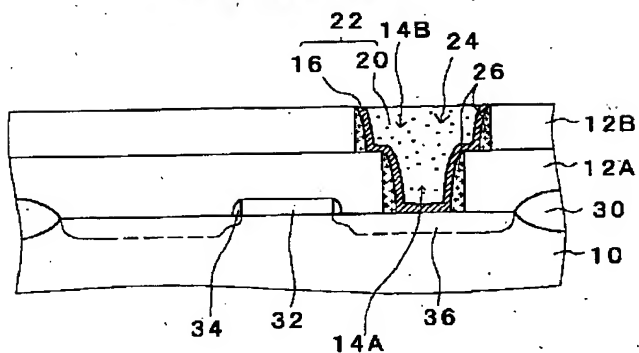
[Drawing 12]

(実施例7の配線構造)



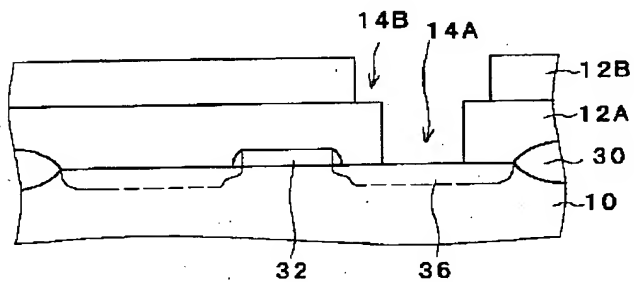
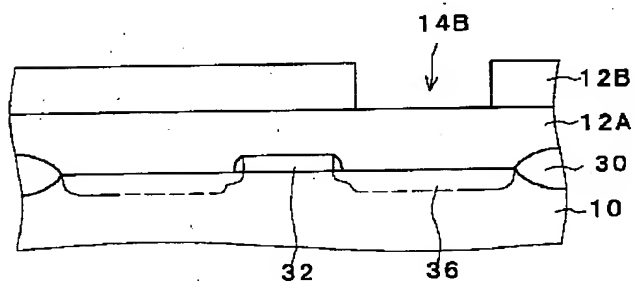
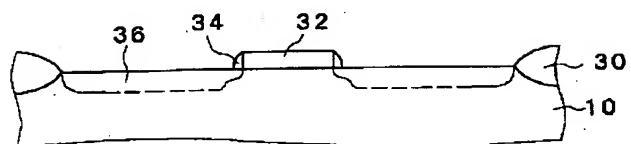
[Drawing 6]

(実施例4の配線構造)



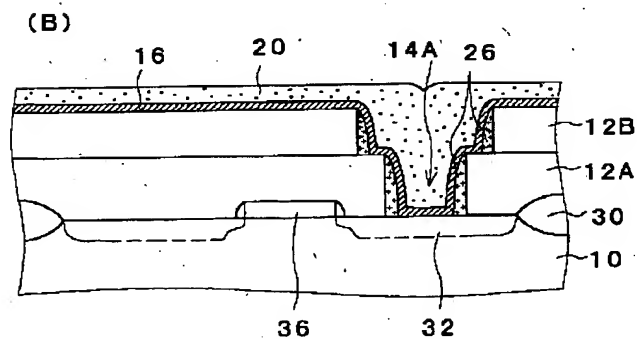
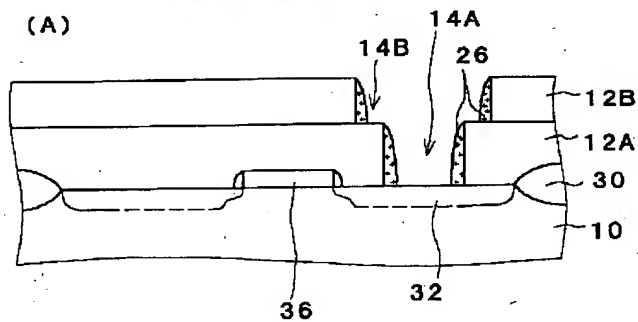
[Drawing 7]

(実施例4の配線形成方法)

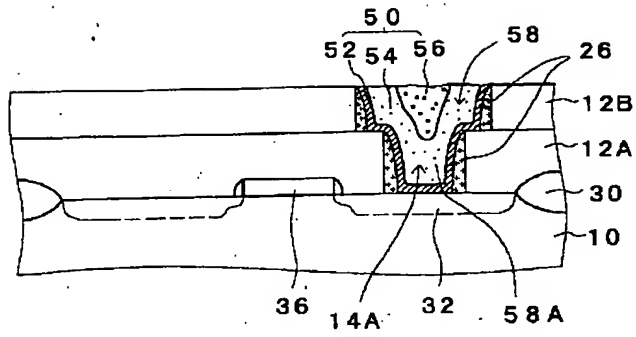


[Drawing 8]

(実施例4の配線形成方法) (続き)

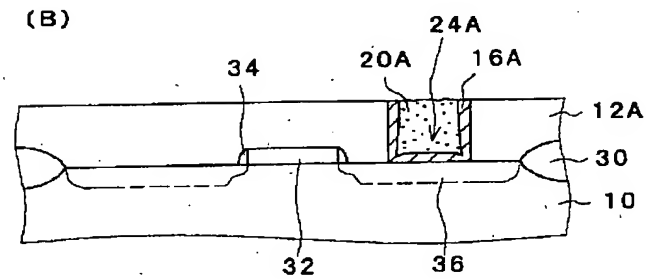
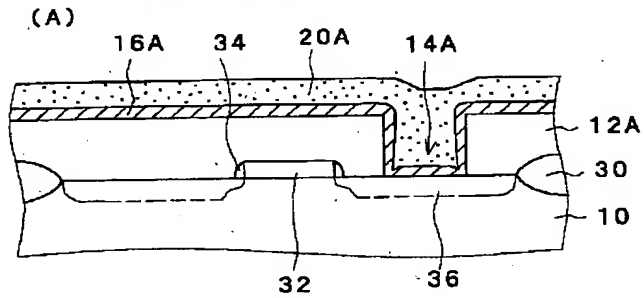


[Drawing 15]



[Drawing 9]

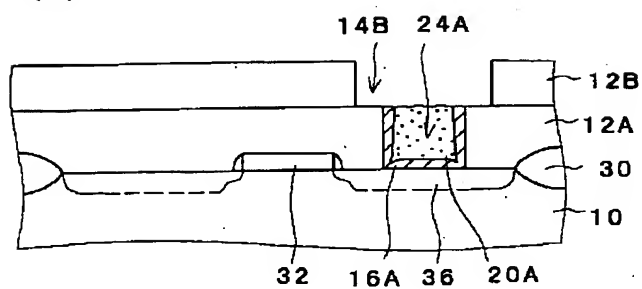
(実施例 5 の配線形成方法)



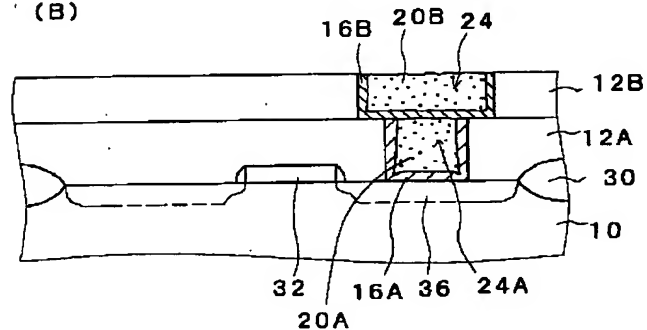
[Drawing 10]

## (実施例 5 の配線形成方法) (続き)

(A)



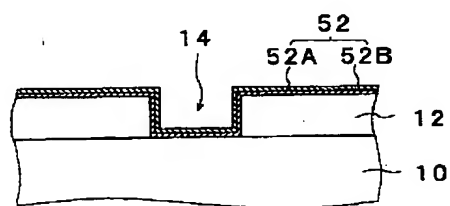
(B)



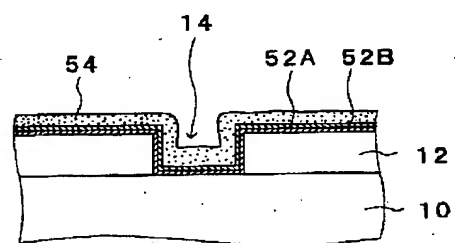
## [Drawing 13]

(実施例 7 の配線形成方法)

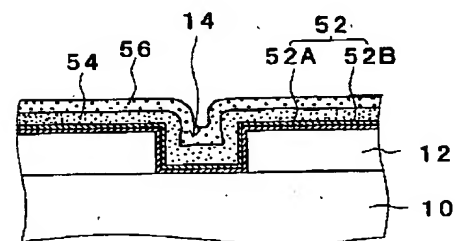
(A)



(B)

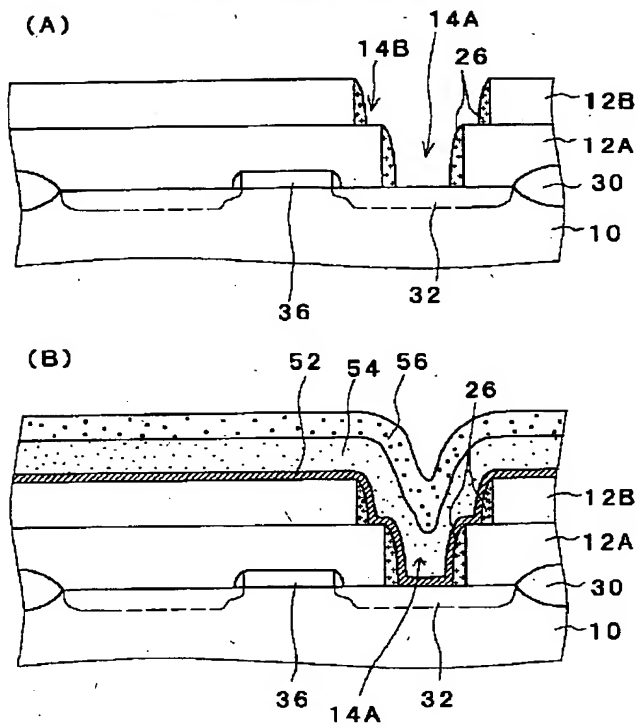


(C)



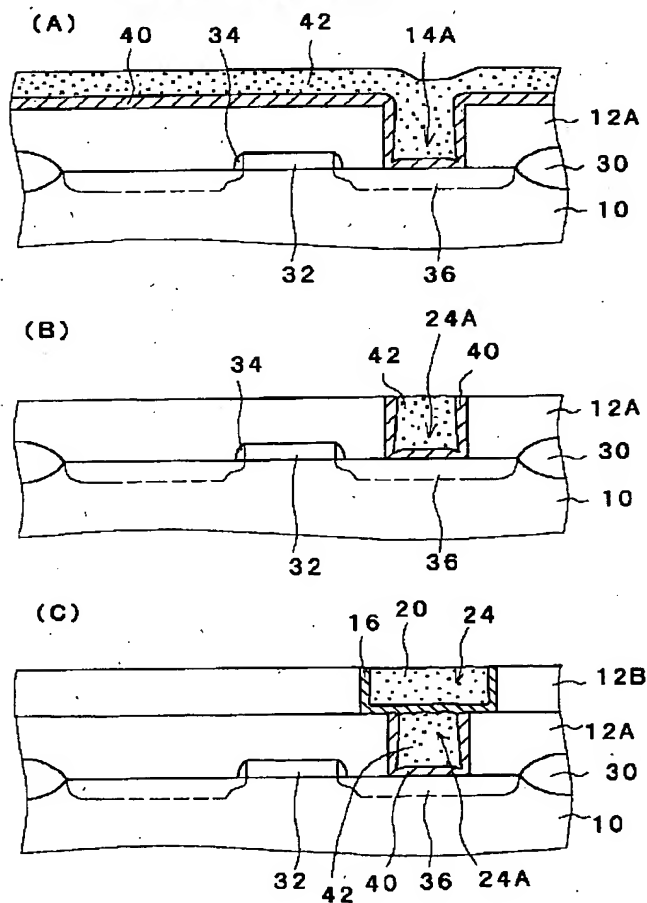
## [Drawing 16]

(実施例 11 の配線形成方法)



[Drawing 11]

(実施例 6 の配線形成方法)

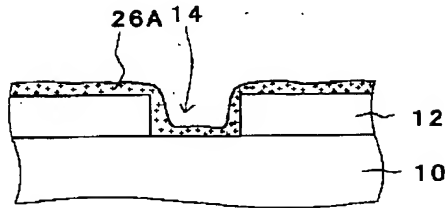


[Drawing 14]

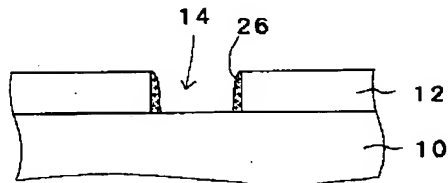


(実施例9の配線形成方法)

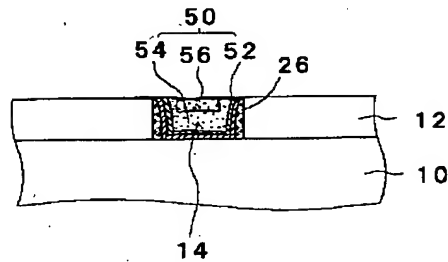
(A)



(B)



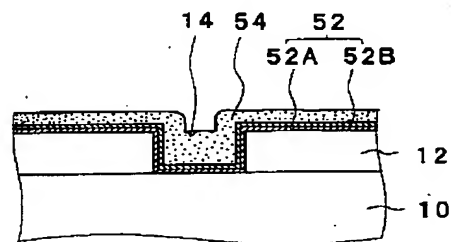
(C)



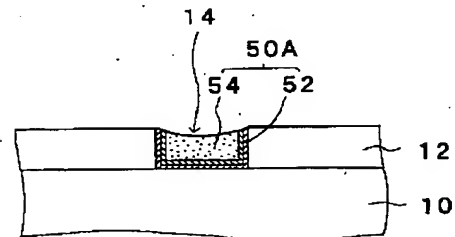
[Drawing 18]

(実施例13の配線形成方法)

(A)

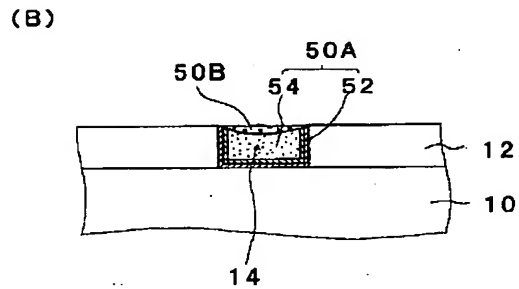
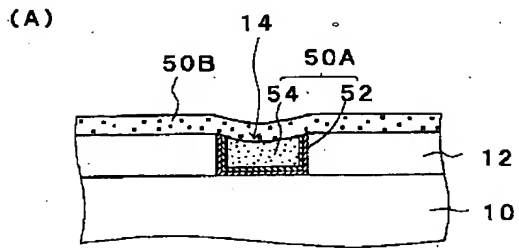


(B)



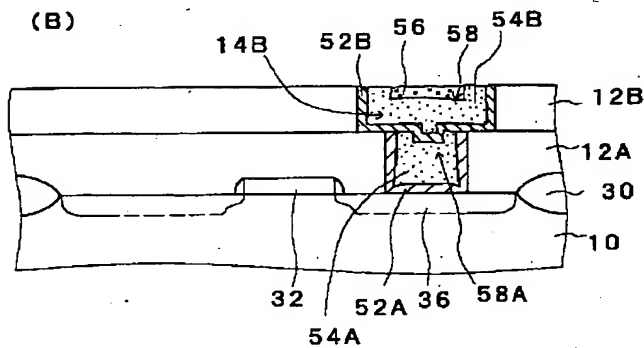
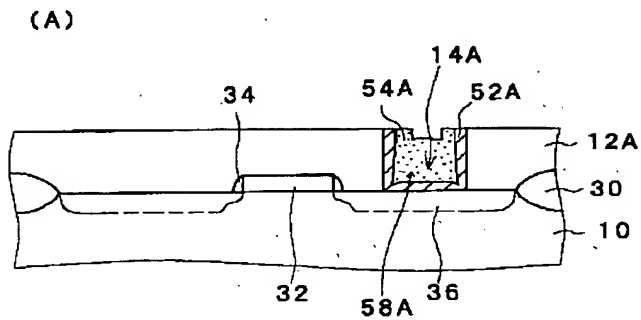
[Drawing 19]

## (実施例 13 の配線形成方法) (続き)



## [Drawing 17]

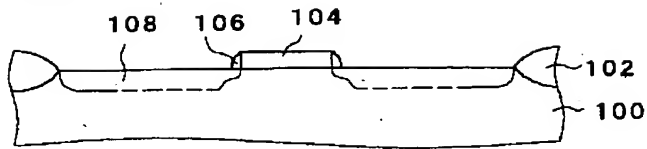
## (実施例 12 の配線形成方法)



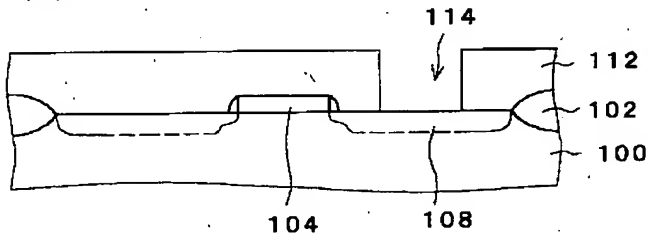
## [Drawing 20]

## (従来技術, その1)

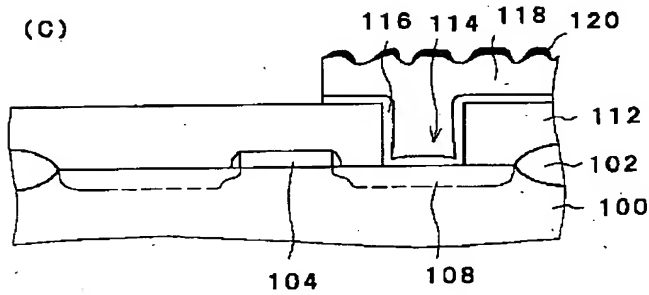
(A)



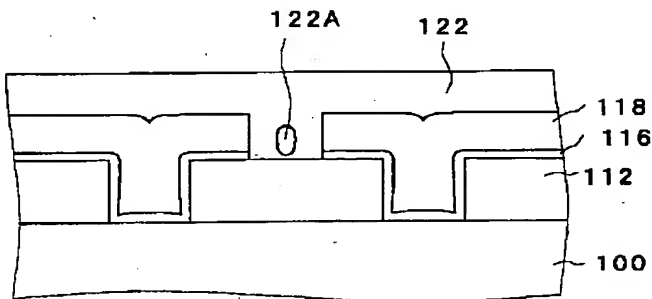
(B)



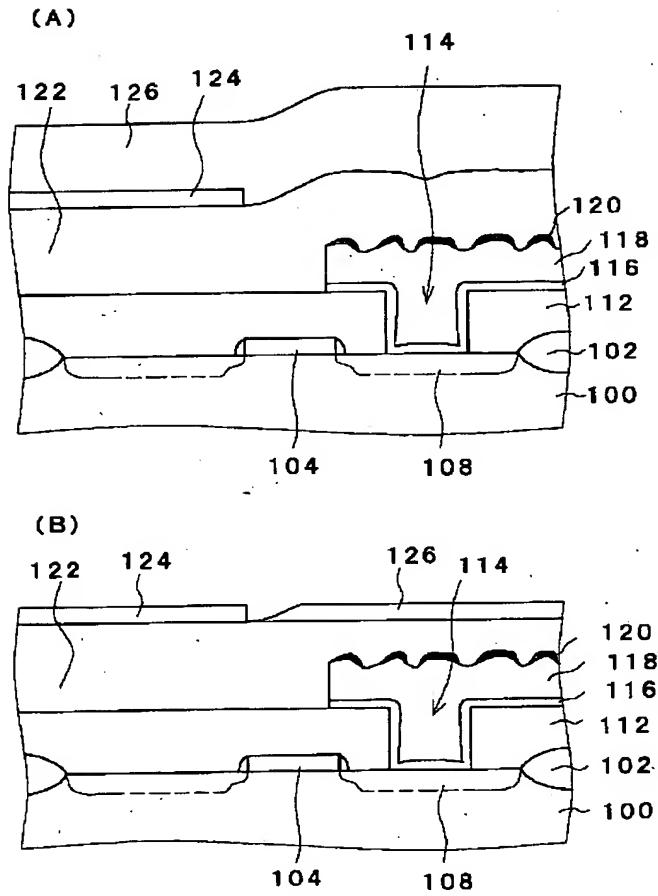
(C)

[Drawing 23]

(従来技術における問題点)

[Drawing 21]

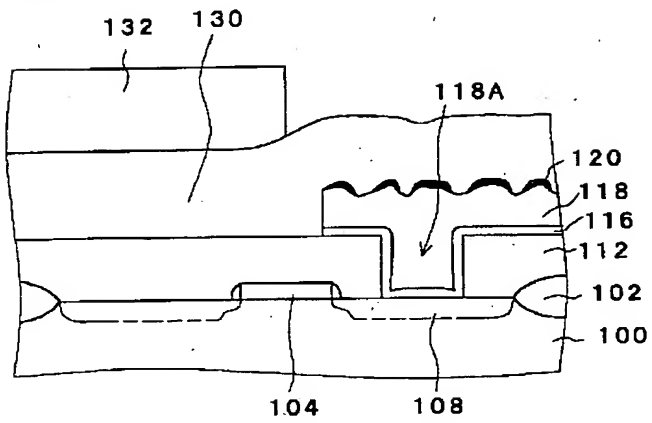
(従来技術, その1) (続き)



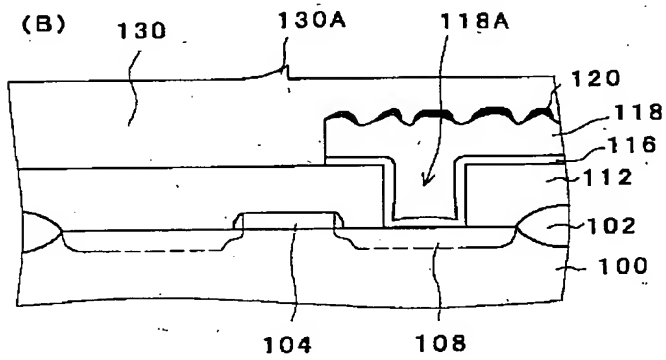
[Drawing 22]

(従来技術, その2)

(A)



(B)



[Translation done.]

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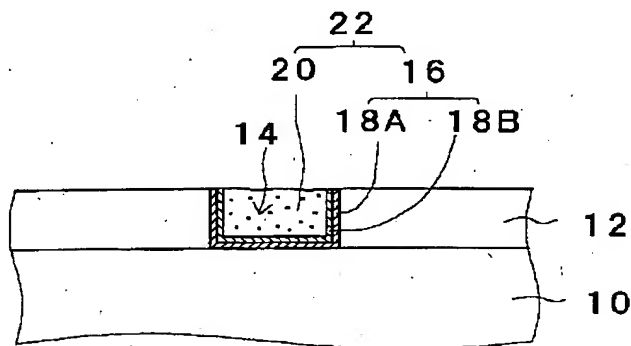
(54) 【発明の名称】 半導体装置の配線構造、配線形成方法、銀薄膜形成方法、CVD装置並びにケミカルメカニカルポリッシュ法

(57) 【要約】

【目的】 配線を形成するためのパターンニング工程を行う必要がなく、しかも、Al系合金やCuを配線材料として用いた場合の問題点を解決できる、新規の半導体装置の配線構造及び配線形成方法を提供する。

【構成】 半導体装置の配線構造は、(イ) 基体10上の絶縁層12に形成された溝部14又は開口部と、(ロ) 溝部14又は開口部内に形成された、下から密着層16層及びAg層20から成る多層22の金属配線層、から構成されている。半導体装置の配線形成方法は、(イ) 基体10上に絶縁層12を形成した後、絶縁層12に溝部14又は開口部を形成し、(ロ) 溝部14又は開口部内を含む絶縁層上に、下から密着層16及びAg層20から成る多層の金属配線層22を形成し、(ハ) 絶縁層12上の金属配線層22を除去し、溝部14又は開口部内に金属配線層22を残す工程から成る。

(実施例1の配線構造)



## 【特許請求の範囲】

【請求項1】 (イ) 基体上の絶縁層に形成された溝部又は開口部と、

(ロ) 該溝部又は開口部内に形成された、下から密着層及びAg層から成る多層の金属配線層、から構成されていることを特徴とする半導体装置の配線構造。

【請求項2】 前記密着層は、Ti層、TiN層、下からTi層/TiN層の2層構造、若しくは下からAg層/Ti層の2層構造から成ることを特徴とする請求項1に記載の半導体装置の配線構造。

【請求項3】 前記溝部又は開口部の側壁に、SiNから成るサイドウォールが形成されていることを特徴とする請求項1又は請求項2に記載の半導体装置の配線構造。

【請求項4】 (イ) 基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

(ロ) 該溝部又は開口部を含む絶縁層上に、下から密着層及びAg層から成る多層の金属配線層を形成する工程と、

(ハ) 絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする半導体装置の配線形成方法。

【請求項5】 前記Ag層の形成は、 $Ag_2CO_3$ 、AgNO<sub>2</sub>、AgBr若しくはAgIを原料として用いた化学気相析出法によることを特徴とする請求項4に記載の半導体装置の配線形成方法。

【請求項6】 前記(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項4又は請求項5に記載の半導体装置の配線形成方法。

【請求項7】 I<sub>2</sub>とKIの混合水溶液を用いてAg層のケミカルメカニカルポリッシュを行うことを特徴とする請求項6に記載の半導体装置の配線形成方法。

【請求項8】 前記(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から成ることを特徴とする請求項4又は請求項5に記載の半導体装置の配線形成方法。

【請求項9】 前記密着層は、Ti層、TiN層、下からTi層/TiN層の2層構造、若しくは下からAg層/Ti層の2層構造から成ることを特徴とする請求項4乃至請求項8のいずれか1項に記載の半導体装置の配線形成方法。

【請求項10】 前記(イ)の工程の後に、溝部又は開口部の側壁にSiNから成るサイドウォールを形成する工程を更に含むことを特徴とする請求項4乃至請求項9のいずれか1項に記載の半導体装置の配線形成方法。

【請求項11】 (イ) 基体上の絶縁層に形成された溝部又は開口部と、

(ロ) 該溝部又は開口部内に形成された、下から密着層、Cu層及びAg層から成る多層の金属配線層、

から構成されていることを特徴とする半導体装置の配線構造。

【請求項12】 前記密着層は、Ti層、TiN層、下からTi層/TiN層の2層構造、若しくは下からAg層/Ti層の2層構造から成ることを特徴とする請求項1に記載の半導体装置の配線構造。

【請求項13】 前記溝部又は開口部の側壁には、SiNから成るサイドウォールが形成されていることを特徴とする請求項11又は請求項12に記載の半導体装置の配線構造。

【請求項14】 前記溝部又は開口部の側壁には、Agから成るサイドウォールが形成されていることを特徴とする請求項11又は請求項12に記載の半導体装置の配線構造。

【請求項15】 (イ) 基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

(ロ) 該溝部又は開口部を含む絶縁層上に、下から密着層、Cu層及びAg層から成る多層の金属配線層を形成する工程と、

(ハ) 絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする半導体装置の配線形成方法。

【請求項16】 前記(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項15に記載の半導体装置の配線形成方法。

【請求項17】 I<sub>2</sub>とKIの混合水溶液を用いてAg層のケミカルメカニカルポリッシュを行うことを特徴とする請求項16に記載の半導体装置の配線形成方法。

【請求項18】 前記(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から成ることを特徴とする請求項15に記載の半導体装置の配線形成方法。

【請求項19】 (イ) 基体上に絶縁層を形成した後、該絶縁層に溝部又は開口部を形成する工程と、

(ロ) 該溝部又は開口部を含む絶縁層上に、下から密着層及びCu層から成る多層の第1の金属配線層を形成する工程と、

(ハ) 絶縁層上の第1の金属配線層を除去し、溝部又は開口部内に第1の金属配線層を残す工程と、

(ニ) 絶縁層上及び第1の金属配線層上に、Ag層から成る第2の金属配線層を形成する工程と、

(ホ) 絶縁層上の第2の金属配線層を除去し、溝部又は開口部内に第2の金属配線層を残す工程、から成ることを特徴とする半導体装置の配線形成方法。

【請求項20】 前記(ハ)の工程における絶縁層上の第1の金属配線層の除去、又は、前記(ホ)の工程における絶縁層上の第2の金属配線層の除去は、ケミカルメカニカルポリッシュ工程から成ることを特徴とする請求項19に記載の半導体装置の配線形成方法。



【請求項 21】 $I_2$ と $KI$ の混合水溶液を用いて $Ag$ 層のケミカルメカニカルポリッシュを行うことを特徴とする請求項 20 に記載の半導体装置の配線形成方法。

【請求項 22】前記 (ハ) の工程における絶縁層上の第 1 の金属配線層の除去、又は、前記 (ホ) の工程における絶縁層上の第 2 の金属配線層の除去は、エッチバック工程から成ることを特徴とする請求項 19 に記載の半導体装置の配線形成方法。

【請求項 23】前記密着層は、 $Ti$ 層、 $TiN$ 層、下から $Ti$ 層/ $TiN$ 層の 2 層構造、若しくは下から $Ag$ 層/ $Ti$ 層の 2 層構造から成ることを特徴とする請求項 15 乃至請求項 22 のいずれか 1 項に記載の半導体装置の配線形成方法。

【請求項 24】前記 (イ) の工程の後に、溝部又は開口部の側壁に $SiN$ から成るサイドウォールを形成する工程を更に含むことを特徴とする請求項 15 乃至請求項 23 のいずれか 1 項に記載の半導体装置の配線形成方法。

【請求項 25】前記 (イ) の工程の後に、溝部又は開口部の側壁に $Ag$ から成るサイドウォールを形成する工程を更に含むことを特徴とする請求項 15 乃至請求項 23 のいずれか 1 項に記載の半導体装置の配線形成方法。

【請求項 26】 $Ag_2CO_3$ を原料として用いた化学気相析出法による銀薄膜の形成方法。

【請求項 27】 $AgNO_2$ を原料として用いた化学気相析出法による銀薄膜の形成方法。

【請求項 28】 $AgBr$ を原料として用いた化学気相析出法による銀薄膜の形成方法。

【請求項 29】 $AgI$ を原料として用いた化学気相析出法による銀薄膜の形成方法。

【請求項 30】原料源と、 $CVD$ チャンバと、原料源と $CVD$ チャンバとを結ぶ配管とを備えた $CVD$ 装置であって、配管を原料の沸点以上に加熱する第 1 のヒーターと、原料を $CVD$ チャンバに導入するための $CVD$ チャンバ導入部を原料の沸点以上に加熱する第 2 のヒーターとを備えていることを特徴とする $CVD$ 装置。

【請求項 31】第 2 のヒーターはランプ加熱装置であることを特徴とする請求項 30 に記載の $CVD$ 装置。

【請求項 32】 $I_2$ 及び $KI$ の混合水溶液を用いて銀薄膜を化学的及び機械的に研磨することを特徴とするケミカルメカニカルポリッシュ法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、 $Ag$  (銀) を配線材料として用いた半導体装置の配線構造及び配線形成方法、銀薄膜形成方法、並びにかかる配線構造の形成に適した $CVD$ 装置及びケミカルメカニカルポリッシュ法に関する。

【0002】

【従来の技術】半導体装置の高集積化に伴い、半導体装置の製造プロセスの寸法ルールが微細化し、これに伴

い、半導体装置における配線幅も微細化してきている。現在、配線材料として、純アルミニウムあるいはアルミニウム合金 (以下、これらを総称して $Al$ 系合金とも呼ぶ) が主に用いられている。そして、例えば、絶縁層から成る下地上に所謂高温アルミニウムスパッタ法にて $Al$ 系合金から成る金属配線層を形成した後、かかる金属配線層をフォトリソグラフィ技術及びエッチング技術によって所望のパターン形状にする。これによって、 $Al$ 系合金から成る配線が形成される。その後、配線上に絶縁膜を形成し、かかる絶縁膜の平坦化処理を行う。

【0003】金属配線層上にフォトリソグラフィ技術によってレジストパターンを形成するためには、露光時、金属配線層による光の乱反射を抑える必要がある。露光時に光の乱反射が抑えられない場合、光の乱反射の影響でハレーションが生じ、形成されたレジストパターンにはレジストの段切れ等の欠陥が生じる。従って、通常、例えば $TiON$ から成る反射防止膜を金属配線層上に形成した後、レジストパターニングを行っている。

【0004】以下、高温アルミニウムスパッタ法及び研磨による平坦化処理法に基づいた従来の半導体素子の製造プロセス例を、図 20、図 21 及び図 22 を参照して説明する。

【0005】【工程-10】半導体基板から成る基体 100 に素子分離領域 102 及びゲート領域 104 を形成する。その後、 $LDD$ イオン注入を行い、ゲートサイドウォール 106 を形成し、イオン注入を行ってソース・ドレイン領域 108 を形成する (図 20 の (A) 参照)。

【0006】【工程-20】その後、全面に層間絶縁層 112 を形成し、次いで、層間絶縁層 112 に開口部 114 を形成する (図 20 の (B) 参照)。

【0007】【工程-30】次に、スパッタ法にて開口部 114 を含む層間絶縁層 112 の全面に $Ti/TiN/Ti$ から成る密着層 116 を形成した後、高温アルミニウムスパッタ法にて $Al$ 系合金 (例えば、 $Al-1wt\%Si$ ) から成る金属配線層 118 を全面に堆積させる。その後、全面に $TiON$ から成る反射防止膜 120 を形成する。そして、反射防止膜 120、金属配線層 118 及び密着層 116 をフォトリソグラフィ技術及びドライエッチング技術によってパターニングすることにより、配線を形成する (図 20 の (C) 参照)。

【0008】【工程-40】次いで、研磨による平坦化処理を施す。即ち、配線を含む層間絶縁層 112 の全面にプラズマ $CVD$ 法にて $SiO_2$ から成る第 1 の絶縁膜 122 を形成し、その上にプラズマ $CVD$ 法にて $SiN$ から成るストッパー層 124 を形成し、更にその上に厚い $SiO_2$ から成る第 2 の絶縁膜 126 を $CVD$ 法にて形成する (図 21 の (A) 参照)。

【0009】【工程-50】その後、上方から第 2 の絶縁膜 126 を研磨する。そしてストッパー層 124 が研

磨面として現れるまで研磨を行う(図21の(B)参照)。こうして、配線の上に平坦化された第1の絶縁膜122を形成する。

【0010】あるいは又、SiNから成るストッパー層124を用いる[工程-40]及び[工程-50]の代わりに、以下の工程にて平坦化处理された絶縁膜を形成することもできる。

【0011】[工程-40'] プラズマCVD法にてSiO<sub>2</sub>から成る絶縁膜130を形成する。

【0012】[工程-50'] その後、絶縁膜130上にレジスト132を形成し、絶縁膜130の凸部が露出するようにレジスト132をパターニングする(図22の(A)参照)。

【0013】[工程-60'] 次に、絶縁膜130の凸部をエッチングした後、レジスト132を除去する(図22の(B)参照)。

【0014】[工程-70'] その後、エッチングされずに残った絶縁膜130の一部分130Aを研磨して、絶縁膜130の平坦化を行う。

【0015】

【発明が解決しようとする課題】配線が微細化すると、目的とする配線幅を制御性良く形成することは困難になる。下地である層間絶縁層112の凹凸の影響を受けて金属配線層118の表面には凹凸が生じる。また、Al系合金から成る金属配線層118を高温アルミニウムスパッタ法等にて形成したとき、金属配線層118の表面は荒れ易い(即ち、凹凸が形成され易い)。これらに起因して、金属配線層118の凹部内における反射防止膜120のカバレッジが低下する(例えば、図20の

(C)参照)。その結果、その部分での光の反射率が低下するために光の乱反射が生じ、結果としてハレーション等の影響で金属配線層118に対して目的のパターニング形状を形成できなくなる。

【0016】また、レジストパターニング後の配線構造は、上からTiONから成る反射防止膜120/金属配線層118である。レジストパターニング後、ドライエッチングによって金属配線層118のパターニングを行う。この場合、通常、エッチングガスとしてBCl<sub>3</sub>系ガスを用いる。ところが、BCl<sub>3</sub>系ガスでのエッチングはケミカル反応のみであり、BCl<sub>3</sub>系ガスによってTiONから成る反射防止膜120をエッチングすることは不可能である。それ故、物理的なスパッタ作用で反射防止膜120をエッチングする必要がある。

【0017】そのため、Al系合金から成る金属配線層118をエッチングする際に、スパッタ作用を有するエッチング条件からケミカルエッチング条件へと変更する必要がある。ところが、反射防止膜120/金属配線層118の膜厚が不均一な場合、このようなエッチング条件の変更により、これらのエッチングが不均一となる。

【0018】更に、SiNから成るストッパー層124

を用いる[工程-40]及び[工程-50]で説明した方法は以下の問題点を有する。即ち、SiO<sub>2</sub>から成る第2の絶縁膜126を研磨する際にストッパー層124を用いているが、SiO<sub>2</sub>とSiNの研磨に対する選択比は3~6程度しか得られない。そのため、SiNから成るストッパー層124が研磨の終点判定を行うべくストッパーとして機能せず、第1の絶縁膜122を研磨し過ぎる場合がある。即ち、制御性良く第2の絶縁膜126を研磨することができない。その結果、第1の絶縁膜122の完全な平坦化が達成できないという問題を有する。

【0019】しかも、CVD法等によってSiO<sub>2</sub>若しくはSOGから成る第1の絶縁膜122で配線間を埋め込む際、配線の間隔が細いと、第1の絶縁膜122の埋め込みが不十分となり、配線間の第1の絶縁膜122に「す(ボイド)」122Aが発生するという問題も有している(図23参照)。

【0020】一方、SiNから成るストッパー層124を用いない[工程-40']~[工程-70']で説明した方法においても、絶縁膜130の研磨時、絶縁膜130の研磨の終点判定を行っていない。このため、絶縁膜130を研磨し過ぎるという問題を有する。

【0021】このように微細な半導体装置の製造においては、配線を形成した後その上に平坦な絶縁膜を形成する従来の方法は上述のような種々の問題点を有しており、これらの問題点を効果的に解決するための方法は未だ無い。

【0022】上記のプロセスにおいては、配線材料としてAl系合金を用いている。Al系合金から成る金属配線層118においては、エレクトロマイグレーションが大きな問題である。また、金属配線層118のドライエッチング時、金属配線層のコロージョンによって金属配線層にボイドが発生し、配線の信頼性低下を招く。特に、微細配線化が進むに従い、配線に電流を流したとき金属配線層118中のアルミニウム粒子が移動する結果、金属配線層に発生した微小な欠けボイドに電流集中が生じる。そのため、エレクトロマイグレーションと欠けボイドの複合作用によって、配線の一層の信頼性低下を招いている。

【0023】かかる問題を解決する一手段として銅(Cu)を配線材料として用いることが提案されている。しかしながら、Cuの適切なエッチング方法が無くCuの加工性が良くないこと、非常に酸化され易く酸素を数%含む炉内での熱処理を行うことができないこと等、種々の問題を有している。加工性の問題は、絶縁層に溝部を形成し、かかる溝部を含む絶縁層上にCuを堆積させた後、絶縁層上のCuをケミカルメカニカルポリッシュ法にて化学的・機械的に研磨することによって回避することができる。しかしながら、溝部に埋め込まれたCuの表面の酸化を防止する有効な手段は知られていない。

【0024】従って、本発明の第1の目的は、配線を形成するためのフォトリソグラフィ技術及びドライエッチング技術による金属配線層のパターニング工程を行う必要がなく、しかも、従来のように配線上に形成された絶縁膜の研磨を行わずに、配線を含む絶縁層の完全なる平坦化を可能とし、更にはA l系合金やC uを配線材料として用いた場合の問題点を解決できる、新規の半導体装置の配線構造及び配線形成方法を提供することにある。

【0025】本発明の第2の目的は、新規の銀薄膜形成方法を提供することにある。更に、本発明の第3の目的は、かかる配線構造及び配線形成方法への適用に適したCVD装置並びにケミカルメカニカルポリッシュ法を提供することにある。

【0026】

【課題を解決するための手段】上記の第1の目的を達成するための本発明の第1の態様に係る半導体装置の配線構造は、(イ)基体上の絶縁層に形成された溝部又は開口部と、(ロ)溝部又は開口部内に形成された、下から密着層及びA g層から成る多層の金属配線層、から構成されていることを特徴とする。

【0027】本発明の第1の態様に係る半導体装置の配線構造においては、密着層を、T i層、T i N層、下からT i層/T i N層の2層構造、若しくは下からA g層/T i層の2層構造から構成することができる。また、溝部又は開口部の側壁に、金属配線層の酸化を防止するために、S i Nから成るサイドウォールを形成してもよい。

【0028】上記の第1の目的を達成するための本発明の第1の態様に係る半導体装置の配線形成方法は、

(イ)基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、(ロ)溝部又は開口部内を含む絶縁層上に、下から密着層及びA g層から成る多層の金属配線層を形成する工程と、(ハ)絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする。

【0029】本発明の第1の態様に係る半導体装置の配線形成方法においては、A g層の形成は、A g<sub>2</sub>CO<sub>3</sub>、A gNO<sub>2</sub>、A gBr若しくはA gIを原料として用いた化学気相析出法にて行うことができる。(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程、あるいは、金属配線層のエッチバック工程から構成することができる。ケミカルメカニカルポリッシュ法においては、I<sub>2</sub>とK Iの混合水溶液を用いてA g層のケミカルメカニカルポリッシュすることができる。

【0030】また、密着層は、T i層、T i N層、下からT i層/T i N層の2層構造、若しくは下からA g層/T i層の2層構造から構成することができる。(イ)の工程の後に、溝部又は開口部の側壁にS i Nから成るサイドウォールを形成する工程を更に含ませることがで

きる。

【0031】上記の第1の目的を達成するための本発明の第2の態様に係る半導体装置の配線構造は、(イ)基体上の絶縁層に形成された溝部又は開口部と、(ロ)溝部又は開口部内に形成された、下から密着層、C u層及びA g層から成る多層の金属配線層、から構成されていることを特徴とする。

【0032】本発明の第2の態様に係る半導体装置の配線構造においては、密着層は、T i層、T i N層、下からT i層/T i N層の2層構造、若しくは下からA g層/T i層の2層構造から構成することができる。また、溝部又は開口部の側壁に、S i Nあるいは又A gから成るサイドウォールを形成してもよい。

【0033】上記の第1の目的を達成するための本発明の第2の態様に係る半導体装置の配線形成方法は、

(イ)基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、(ロ)溝部又は開口部内を含む絶縁層上に、下から密着層、C u層及びA g層から成る多層の金属配線層を形成する工程と、(ハ)絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残す工程、から成ることを特徴とする。

【0034】本発明の第2の態様に係る半導体装置の配線形成方法においては、(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のケミカルメカニカルポリッシュ工程から構成することができる。この場合、ケミカルメカニカルポリッシュによるA g層の除去は、I<sub>2</sub>とK Iの混合水溶液を用いて行う。あるいは又、(ハ)の工程における絶縁層上の金属配線層の除去は、金属配線層のエッチバック工程から構成することができる。

【0035】上記の第1の目的を達成するための本発明の第3の態様に係る半導体装置の配線形成方法は、

(イ)基体上に絶縁層を形成した後、絶縁層に溝部又は開口部を形成する工程と、(ロ)溝部又は開口部内を含む絶縁層上に、下から密着層及びC u層から成る多層の第1の金属配線層を形成する工程と、(ハ)絶縁層上の第1の金属配線層を除去し、溝部又は開口部内に第1の金属配線層を残す工程と、(ニ)絶縁層上及び第1の金属配線層上に、A g層から成る第2の金属配線層を形成する工程と、(ホ)絶縁層上の第2の金属配線層を除去し、溝部又は開口部内に第2の金属配線層を残す工程、から成ることを特徴とする。

【0036】本発明の第3の態様に係る半導体装置の配線形成方法においては、(ハ)の工程における絶縁層上の第1の金属配線層の除去、又は、(ホ)の工程における絶縁層上の第2の金属配線層の除去は、ケミカルメカニカルポリッシュ工程から構成することができる。この場合、ケミカルメカニカルポリッシュによるA g層の除去は、I<sub>2</sub>とK Iの混合水溶液を用いて行う。あるいは又、(ハ)の工程における絶縁層上の第1の金属配線層

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の除去、又は、(ホ)の工程における絶縁層上の第2の金属配線層の除去は、エッチバック工程から構成することができる。

【0037】本発明の第2又は第3の態様に係る半導体装置の配線形成方法においては、密着層は、Ti層、TiN層、下からTi層/TiN層の2層構造、若しくは下からAg層/Ti層の2層構造から構成することができる。また、(イ)の工程の後に、溝部又は開口部の側壁にSiNあるいはAgから成るサイドウォールを形成する工程を更に含むことができる。

【0038】上記の第2の目的を達成するための銀薄膜の形成方法は、 $Ag_2CO_3$ を原料として用いた化学気相析出法によることを特徴とする。あるいは又、 $AgNO_2$ を原料として用いた化学気相析出法によることを特徴とする。更には、 $AgBr$ を原料として用いた化学気相析出法によることを特徴とする。更には、 $AgI$ を原料として用いた化学気相析出法によることを特徴とする。これらの原料をガス化して不活性ガス等のキャリアガスを用いてCVDガスとして用いる。

【0039】上記の第3の目的を達成するための本発明のCVD装置は、原料源と、CVDチャンバと、原料源とCVDチャンバとを結ぶ配管とを備えている。そして、配管を原料の沸点以上に加熱する第1のヒーターと、原料をCVDチャンバに導入するためのCVDチャンバ導入部を原料の沸点以上に加熱する第2のヒーターとを備えていることを特徴とする。第2のヒーターをランプ加熱装置とすることができる。

【0040】上記の第3の目的を達成するためのケミカルメカニカルポリッシュ法は、 $I_2$ 及び $KI$ の混合水溶液を用いて銀薄膜を化学的及び機械的に研磨することを

特徴とする。

【0041】

【作用】本発明においては、溝部又は開口部内に金属配線層が形成されている。このような形態の金属配線層は、絶縁層上の金属配線層を除去し、溝部又は開口部内に金属配線層を残すことによって形成されるので、従来技術のようにフォトリソグラフィ技術及びドライエッチング技術によって絶縁層上に形成された金属配線層のパターニングを行う必要がない。また、絶縁層上の金属配線層の除去による平坦化処理を行うので、従来の技術のような配線の上に形成された絶縁膜の平坦化処理を行う必要がない。

【0042】 $Ag$ は高温熱処理で酸化され難い。 $Ag$ も酸化するが $100^\circ C$ 以上の温度で $AgO \rightarrow Ag + O$ に分解する。このため数百 $^\circ C$ の温度で $AgO$ は安定化せず、 $Ag$ の酸化物を保たない。また、 $Ag$ から金属配線層を構成するので、 $Al$ 系合金のようなエレクトロマイグレーションの問題は発生しない。従って、本発明の第1の態様に係る配線構造あるいは配線形成方法においては、安定した配線を形成することができる。

【0043】本発明の第2の態様に係る配線構造あるいは第2又は第3の態様に係る配線形成方法においては、 $Ag$ 層及び $Cu$ 層から金属配線層を構成するので、 $Al$ 系合金のようなエレクトロマイグレーションの問題は発生しない。しかも、 $Cu$ 層の表面は $Ag$ 層で被覆されているので、 $Cu$ 層の酸化を防止することができる。

【0044】以下、図面を参照して、実施例に基づき本発明を説明する。尚、実施例1～実施例6においては、本発明の第1の態様に係る半導体装置の配線構造及び第1の態様に係る配線形成方法を説明する。また、実施例7～実施例12においては、本発明の第2の態様に係る半導体装置の配線構造及び第2の態様に係る配線形成方法を説明する。更に、実施例13～実施例15においては、本発明の第2の態様に係る半導体装置の配線構造及び第3の態様に係る配線形成方法を説明する。

【0045】(実施例1) 実施例1～実施例6は、本発明の第1の態様に係る半導体装置の配線構造及び第1の態様に係る配線形成方法に関する。図1に半導体装置の模式的な一部断面図を示すように、実施例1の配線構造は、基体10上の絶縁層12に形成された溝部14、溝部14内に形成された多層の金属配線層22から成る。金属配線層22は、下から密着層16及び $Ag$ 層20から構成されている。密着層16は、下からTi層18A/TiN層18Bの2層構造である。

【0046】実施例1の配線形成方法は、(イ)基体10上に絶縁層12を形成した後、絶縁層12に溝部14を形成する工程と、(ロ)溝部14内を含む絶縁層12上に、下から密着層16及び $Ag$ 層20から成る多層の金属配線層22を形成する工程と、(ハ)絶縁層12上の金属配線層22を除去し、溝部14内に金属配線層22を残す工程から成る。 $Ag$ 層20の形成は、 $Ag_2CO_3$ を原料として用いた化学気相析出法による。また、(ハ)の工程における絶縁層12上の金属配線層22の除去は、 $I_2$ と $KI$ の混合水溶液を用いた金属配線層22のケミカルメカニカルポリッシュ工程から成る。 $SiO_2$ から成る絶縁層12をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する金属配線層22と絶縁層12の選択比を無限大まで設定することが可能となる。

【0047】以下、半導体装置等の模式的な一部断面図である図2を参照して、実施例1の配線形成方法を具体的に説明する。

【0048】[工程-100] 例えば半導体基板から成る基体10上に $SiO_2$ から成る絶縁層12を形成する。絶縁層12の形成条件を、例えば以下のとおりとすることができる。

使用ガス :  $SiH_4/O_2/N_2 = 250/250/1000$  sccm

基板加熱温度 :  $420^\circ C$

圧力 : 13.3 Pa

膜厚 : 0.8 μm

【0049】【工程-110】その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層12に溝部14を形成する(図2の(A)参照)。尚、溝部14は図2の紙面に垂直な方向に延びている。ドライエッチングの条件を、例えば以下のとおりとすることができる。

使用ガス : C<sub>4</sub>F<sub>8</sub>=50 sccm

RFパワー : 1200 W

圧力 : 2 Pa

【0050】【工程-120】次に、下からTi層18A/TiN層18Bから成る密着層16を溝部14を含む絶縁層12上にスパッタ法にて形成する(図2の(B)参照)。密着層16を、例えば以下の条件で形成することができる。

Ti層18Aの形成

使用ガス : Ar=100 sccm

パワー : 4 kW

圧力 : 0.47 Pa

成膜温度 : 150° C

膜厚 : 50 nm

TiN層18Bの形成

使用ガス : Ar/N<sub>2</sub>=40/70 sccm

パワー : 5 kW

圧力 : 0.47 Pa

膜厚 : 70 nm

【0051】【工程-130】その後、銀(Ag)層20をCVD法にて全面に形成する(図2の(C)参照)。Ag層20の形成は、Ag<sub>2</sub>CO<sub>3</sub>を原料として用いた化学気相析出法による。CVDの条件を、例えば以下のとおりとすることができる。

原料 : Ag<sub>2</sub>CO<sub>3</sub>

原料源温度 : 170° C

使用ガス : Ag<sub>2</sub>CO<sub>3</sub>/Ar/H<sub>2</sub>=10/25/1000 sccm

圧力 : 2.6×10<sup>3</sup> Pa

基板加熱温度 : 450° C

これによって、溝部14内を含む絶縁層12上にAg層20が堆積する。Ag層20は下記の反応によって形成される。



【0052】Ag層20の形成のために、図3に示す本発明のCVD装置を使用した。このCVD装置は、CVDチャンバ200と、原料源202と、原料源とCVDチャンバとを結ぶ配管204とを備えている。そして、配管204を原料の沸点以上に加熱する第1のヒーター206と、原料をCVDチャンバに導入するためのCVDチャンバ導入部208を原料の沸点以上に加熱する第2のヒーター210とを備えている。第2のヒーター210はランプ加熱装置であり、ミラー212が設けられ

ている。また、第2のヒーター210と対抗するCVDチャンバ導入部208近傍の配管204の部分には石英製の窓214が設けられている。尚、図3中、216は基板10を加熱するためのランプ加熱装置、218は不活性ガス導入部、220は原料源202を加熱するためのヒーターである。第1及び第2のヒーター206、210によって、配管204及びCVDチャンバ導入部208内を流れるAg<sub>2</sub>CO<sub>3</sub>ガスは沸点である218° C以上に保持される。

【0053】【工程-140】次に、ケミカルメカニカルポリッシュ法によって絶縁層12上のAg層20及び密着層16を化学的及び機械的に研磨して除去し、溝部14内にAg層20及び密着層16を残し、金属配線層22から成る配線を形成する(図1参照)。ケミカルメカニカルポリッシュには、図4に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、例えば以下のとおりとすることができる。

研磨プレート回転数 : 3.7 rpm

基板保持台回転数 : 17 rpm

20 研磨圧力 : 5.5×10<sup>8</sup> Pa

パッド温度 : 40° C

I<sub>2</sub>+KIの混合水溶液を用いて、ケミカルメカニカルポリッシュを行う。

【0054】従来SiO<sub>2</sub>を研磨する場合はスラリー(SiO<sub>2</sub>系の研磨剤+KOH+水)を用いるが、スラリーでSiO<sub>2</sub>を研磨する際、スラリーが研磨すべき面内に均一に分布しないため、研磨し過ぎ等により基板内の研磨面の平坦化にばらつきが生じるという問題がある。Ag層20及び密着層16を研磨する場合、スラリーを必要とせず、I<sub>2</sub>+KIの混合水溶液で研磨することで、Ag層20及び密着層16のみを除去することが可能であり、基板内の研磨面の平坦化にばらつきも少ないという利点を有する。

【0055】これによって、平坦な絶縁層12に埋め込まれた金属配線層22から成る配線が形成される。実施例1においては、従来の配線形成方法のように金属配線層のレジストパターニング処理及びドライエッチング処理が不要となり、レジストパターニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。

【0056】(実施例2) 実施例1では、絶縁層12上のAg層20及び密着層16から成る金属配線層22の除去をケミカルメカニカルポリッシュ法にて行った。実施例2においては、その代わりに、ドライエッチングによるエッチバック法にて金属配線層22を除去する。尚、その他の工程は実施例1と同様であり、詳細な説明は省略する。

【0057】【金属配線層22のエッチング工程】溝部14を含む絶縁層12上に形成されたAg層20及び密

着層16を、例えば以下の条件のドライエッチング法にてエッチバックし、溝部14内に密着層16及びAg層20から成る金属配線層22を残す。

使用ガス :  $\text{NO}_2/\text{O}_2=20/20\text{ sccm}$   
 マイクロ波パワー : 850W  
 RFパワー : 10W  
 圧力 : 1.3Pa  
 基板加熱温度 : 100°C

【0058】(実施例3) 実施例3においては、実施例1の【工程-110】と【工程-120】との間に、溝部14の側壁にSiNから成るサイドウォール26を形成する工程を更に含む。尚、その他の工程は実施例1と同様であり、詳細な説明は省略する。以下、実施例3のサイドウォール26の形成工程を、図5を参照して説明する。サイドウォール26を形成することによって、絶縁層12による密着層16の酸化を防止することができる。

【0059】[サイドウォール26の形成工程] 溝部14内を含む絶縁層12上の全面にプラズマCVD法にてSiN層26Aを堆積させる(図5の(A)参照)。SiN層26Aの形成条件を、以下に例示する。

使用ガス :  $\text{SiH}_4/\text{NH}_3/\text{N}_2=180/500/720\text{ sccm}$   
 温度 : 200°C  
 圧力 : 40Pa  
 膜厚 : 100nm

【0060】その後、SiN層26Aを全面エッチバックする(図5の(B)参照)。エッチバックの条件を、例えば以下のとおりとすることができる。

使用ガス :  $\text{CHF}_3=50\text{ sccm}$   
 RFパワー : 300W  
 圧力 : 2Pa

これによって、溝部14の側壁にサイドウォール26が形成される。以降、実施例1の【工程-120】～【工程-140】を経て、図5の(C)に示す配線構造を形成することができる。

【0061】(実施例4) 図6に模式的な一部断面図を示す実施例4の配線構造は、実施例1と若干異なり、半導体基板から成る基体10上の第1の絶縁層12Aに形成された開口部14Aと、第1の絶縁層12A上に形成された第2の絶縁層12Bに形成された溝部14Bと、開口部14A及び溝部14Bに埋め込まれた密着層16及びAg層20から成る金属配線層22から構成されている。この場合、開口部14Aの側壁及び溝部14Bの側部にSiNから成るサイドウォール26を形成してもよい。また、開口部14Aを金属配線層22で埋め込むことによって、下層導体層(例えば、ソース・ドレイン領域36)と溝部14B内の配線24とが電氣的に接続される。

【0062】実施例4の配線形成方法は、実施例1と若

干異なり、予め半導体基板から成る基体10上の第1の絶縁層12Aに開口部14Aを、また、第1の絶縁層12A上に形成された第2の絶縁層12Bに溝部14Bを形成した後、密着層16及びAg層20から成る金属配線層22で開口部14A及び溝部14Bを埋め込み配線構造を形成する。第2の絶縁層12B上の金属配線層22はケミカルメカニカルポリッシュ法にて除去される。以下、半導体装置等の模式的な一部断面図である図7及び図8を参照して、実施例4の配線形成方法を説明する。

【0063】[工程-400] Si(100)から成る半導体基板から成る基体10上に、通常の方法で素子分離領域30及びゲート領域32を形成する。次いで、LDDイオン注入を行った後、全面にゲートサイドウォール34を形成するためにSiO<sub>2</sub>膜を堆積させる。SiO<sub>2</sub>膜の堆積条件を、例えば以下のとおりとすることができる。

使用ガス :  $\text{SiH}_4/\text{O}_2/\text{N}_2=250/250/100\text{ sccm}$   
 温度 : 420°C  
 圧力 : 13.3Pa  
 膜厚 : 0.25μm

更に、SiO<sub>2</sub>膜の全面エッチバックを行い、ゲート領域32の側壁にゲートサイドウォール34を形成する。全面エッチバックを、例えば以下の条件で行うことができる。

使用ガス :  $\text{C}_4\text{F}_8=50\text{ sccm}$   
 RFパワー : 1200W  
 圧力 : 2Pa

その後、ソース・ドレイン領域36の形成のために、不純物イオン注入を、例えば以下の条件にて行う。

N型チャネルの形成  
 $\text{As } 20\text{ KeV}, 5 \times 10^{15}/\text{cm}^2$   
 P型チャネルの形成  
 $\text{BF}_2 \ 20\text{ KeV}, 3 \times 10^{15}/\text{cm}^2$

こうして、図7の(A)に模式的な一部断面図で示す構造を得ることができる。

【0064】[工程-410] その後、SiO<sub>2</sub>及びBPSGの2層から成る第1の絶縁層12Aを、例えば以下の条件のCVD法にて全面に形成する。

SiO<sub>2</sub>層の形成  
 使用ガス : TEOS 50 sccm  
 圧力 : 40Pa  
 温度 : 720°C  
 膜厚 : 400nm

BPSG層の形成  
 使用ガス :  $\text{SiH}_4/\text{PH}_3/\text{B}_2\text{H}_6/\text{O}_2/\text{N}_2=80/7/7/1000/32000\text{ sccm}$   
 温度 : 400°C  
 圧力 :  $1.0 \times 10^5\text{ Pa}$

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膜厚 : 500 nm

更に900°C、20分のリフロー処理を行い、第1の絶縁層12Aの平坦化を行う。

【0065】【工程-420】次に、SiO<sub>2</sub>から成る第2の絶縁層12Bを全面に形成する。第2の絶縁層12Bを、例えば以下の条件で形成することができる。

使用ガス : SiH<sub>4</sub>/O<sub>2</sub>/N<sub>2</sub>=250/250/100 sccm

温度 : 420°C

圧力 : 1.3, 3 Pa

膜厚 : 0.8 μm

【0066】【工程-430】その後、実施例1の【工程-110】と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第2の絶縁層12Bに溝部14Bを形成する(図7の(B)参照)。

【0067】【工程-440】次いで、レジストパターニング後ドライエッチングを行うことによって、第1の絶縁層12Aに開口部14Aを形成する(図7の(C)参照)。ここで、溝部14Bの幅を開口部14Aの径よりも大きくする。ドライエッチングの条件を、例えば以

下のとおりとすることができる。

使用ガス : C<sub>4</sub>F<sub>8</sub> 50 sccm

RFパワー : 1200 W

圧力 : 2 Pa

更に、開口部内にイオン注入を行うことにより、接合領域を形成した後、1100°C、10秒の活性化アニールを行う。イオン注入の条件として、以下の例を挙げることができる。

N型チャネルの形成

As 20 KeV, 5×10<sup>15</sup>/cm<sup>2</sup>

P型チャネルの形成

BF<sub>2</sub> 20 KeV, 3×10<sup>15</sup>/cm<sup>2</sup>

【0068】【工程-450】その後、実施例3の【サイドウォール26の形成工程】と同様に、全面にプラズマCVD法にてSiN層を形成し、次いで、SiN層を全面エッチバックして、開口部14Aの側壁及び溝部14Bの側壁にSiNから成るサイドウォール26を形成することが望ましい(図8の(A)参照)。

【0069】【工程-460】次に、下からTi層/TiN層から成る密着層16を開口部14A及び溝部14Bを含む第2の絶縁層12B上にスパッタ法にて形成する。この工程は、実施例1の【工程-120】と同様とすることができる。

【0070】【工程-470】その後、実施例1の【工程-130】と同様に、Ag<sub>2</sub>CO<sub>3</sub>を原料として用いた化学気相析出法によって、Ag層20を全面に形成する(図8の(B)参照)。

【0071】【工程-480】次に、実施例1の【工程-140】と同様に、ケミカルメカニカルポリッシュ法によって第2の絶縁層12B上のAg層20及び密着層

16を化学的及び機械的に研磨して除去し、溝部14B内及び開口部14A内にAg層20及び密着層16を残し、金属配線層22から成る接続孔及び配線を形成する(図6参照)。即ち、開口部14A内に金属配線層22が埋め込まれた接続孔(例えば、所謂コンタクトホール)が形成される。また、溝部14Bに金属配線層22が埋め込まれた配線24が形成される。

【0072】尚、Ag層20及び密着層16から成る金属配線層22をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例2と同様にドライエッチング法にてエッチバックすることで除去することもできる。

【0073】(実施例5) 実施例5は、実施例4の変形である。実施例5の配線構造は実施例4と同様であるが、配線形成方法が実施例4と相違する。即ち、第1の絶縁層12Aに設けられた開口部14AをAgから成る金属配線材料で埋め込み接続孔24Aを完成させ、次いで、その上に第2の絶縁層12Bを堆積させ、かかる第2の絶縁層12Bに溝部14Bを形成する点が実施例4と相違する。実施例5においては、実施例4の【工程-400】、【工程-410】及び【工程-440】は同様の工程であり、その他の工程が異なる。以下、図9及び図10を参照して、実施例5の方法を説明する。

【0074】

【工程-500】～【工程-520】Si(100)の半導体基板から成る基体10上に、通常の方法で素子分離領域30及びゲート領域32を形成する。次いで、LDDイオン注入を行った後、ゲートサイドウォール34を形成し、ソース・ドレイン領域36の形成のために、不純物イオン注入を行う。その後、SiO<sub>2</sub>及びBPSGの2層から成る第1の絶縁層12Aを、例えばCVD法にて全面に形成し、リフロー処理を行い、第1の絶縁層12Aの平坦化を行う。次いで、第1の絶縁層12Aに、レジストパターニング後ドライエッチングにて開口部14Aを形成し、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。これらの工程は、実施例4の【工程-400】、【工程-410】及び【工程-440】と同様とすることができる。次いで、SiNから成るサイドウォール(図示せず)を開口部14Aの側壁に形成してもよい。

【0075】【工程-530】

【工程-520】の後、実施例1の【工程-120】と同様の方法で、下からTi/TiNから成る第1の密着層16Aを全面に形成する。次いで、実施例1の【工程-130】と同様の方法で、第1のAg層20AをCVD法にて全面に成膜し、第1の密着層16Aと第1のAg層20Aから成る第1の金属配線層を形成する(図9の(A)参照)。

【0076】【工程-540】その後、ケミカルメカニカルポリッシュ法にて第1の絶縁層12A上の第1の金属配線層を除去し、開口部14A内のみに第1の金属配

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線層20A, 16Aを残す(図9の(B)参照)。ケミカルメカニカルポリッシュの条件は、実施例1の【工程-140】と同様とすることができる。これによって、開口部14Aに第1の金属配線層が埋め込まれた所謂コンタクトホール24Aが形成される。ケミカルメカニカルポリッシュ法の代わりに、実施例2と同様に、ドライエッチング法によるエッチバックにて開口部14A内のみに第1の金属配線層20A, 16Aを残してもよい。

【0077】【工程-550】次いで、全面にSiO<sub>2</sub>から成る第2の絶縁層12Bを形成する。第2の絶縁層12Bを、例えば実施例4の【工程-420】と同様の条件で形成することができる。その後、実施例4の【工程-430】と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第2の絶縁層12Bに溝部14Bを形成する(図10の(A)参照)。その後、必要に応じて、実施例4の【工程-450】と同様に、全面にプラズマCVD法にてSiN層を形成し、次いで、SiN層を全面エッチバックし、これによって、溝部14Bの側壁にSiNから成るサイドウォール(図示せず)を形成してもよい。

【0078】【工程-560】次に、実施例1の【工程-120】と同様の方法で、厚さ30nmのTiから成る第2の密着層16Bを溝部14Bを含む第2の絶縁層12B上にスパッタ法にて形成した後、実施例1の【工程-130】と同様の方法で、第2のAg層20BをCVD法にて全面に成膜し、第2の密着層16Bと第2のAg層20Bから成る第2の金属配線層を形成する。

【0079】【工程-570】次いで、ケミカルメカニカルポリッシュ法によって第2の絶縁層12B上の第2の金属配線層20B, 16Bを除去し、溝部14B内に第2のAg層20B及び第2の密着層16Bを残し、配線24を形成する(図10の(B)参照)。ケミカルメカニカルポリッシュの条件は、実施例1の【工程-140】と同様とすることができる。

【0080】尚、ケミカルメカニカルポリッシュ法によって第2の絶縁層12B上の第2の金属配線層20B, 16Bを除去する代わりに、実施例2と同様に、第2の金属配線層20B, 16Bをドライエッチング法にてエッチバックし、これによって、溝部14B内にのみ第2の金属配線層20B, 16Bを残し、溝部14B内に配線24を形成することもできる。

【0081】(実施例6) 実施例6は実施例5の変形である。実施例6が実施例5と相違する点は、予め開口部14A内にCVD法にてタングステンプラグを形成する点にある。以下、図11を参照して実施例6の配線形成方法を説明する。

【0082】

【工程-600】～【工程-620】これらの工程は、実施例5の【工程-500】～【工程-520】と同様とすることができる。

【0083】【工程-630】

【工程-620】の後、Ti/TiNから成るバリア層40を全面にスパッタ法にて形成し、その後、全面にタングステン層42をCVD法にて成膜する(図11の(A)参照)。Ti及びTiNの成膜条件を、例えば実施例1の【工程-120】と同様とすることができる。また、CVD法によるタングステンの成膜条件を、以下に例示する。

使用ガス : WF<sub>6</sub>/H<sub>2</sub>=95/550sccm

成膜温度 : 450°C

圧力 : 1.1×1.04Pa

膜厚 : 0.4μm

【0084】【工程-640】その後、ドライエッチング法にてエッチバックを行い、第1の絶縁層12A上のタングステン層42及びバリア層40を除去して、開口部14A内のみにタングステン層42から成るメタルプラグ及びバリア層40を残す(図11の(B)参照)。ドライエッチングの条件は、例えば以下のとおりとすることができる。

20 使用ガス : SF<sub>6</sub>=50sccm

マイクロ波パワー : 850W

RFパワー : 150W

圧力 : 1.33Pa

これによって、開口部14Aにタングステンが埋め込まれた所謂タングステンプラグから成るコンタクトホール24Aが形成される。尚、ドライエッチング法によるエッチバックの代わりに、ケミカルメカニカルポリッシュ法によって開口部14A内のみにタングステン層42及びバリア層40を残してもよい。

30 【0085】【工程-650】次いで、全面にSiO<sub>2</sub>から成る第2の絶縁層12Bを形成する。第2の絶縁層12Bを、例えば実施例5の【工程-550】と同様の条件で形成することができる。その後、実施例5の【工程-550】と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第2の絶縁層12Bに溝部14Bを形成する。尚、溝部14Bの幅を開口部14Aの径よりも大きくする。

【0086】【工程-660】次に、実施例5の【工程-560】と同様の方法で、30nm厚さのTiから成る密着層16を溝部14Bを含む第2の絶縁層12B上にスパッタ法にて形成した後、実施例1の【工程-130】と同様の方法で、Ag層20をCVD法にて全面に成膜し、密着層16とAg層20から成る金属配線層を形成する。

【0087】【工程-670】その後、実施例1の【工程-140】と同様の方法で、第2の絶縁層12B上の金属配線層をケミカルメカニカルポリッシュ法あるいはドライエッチングによるエッチバックにて除去する。これによって、溝部14B内にのみ金属配線層を残し、溝部14B内に密着層16及びAg層20から成る金属配

線層から構成された配線 2 4 を形成する ( 図 1 1 の ( C ) 参照 )。

【 0 0 8 8 】 ( 実施例 7 ) 実施例 7 ~ 実施例 1 2 は、本発明の第 2 の態様に係る半導体装置の配線構造及び第 2 の態様に係る配線形成方法に関する。図 1 2 に半導体装置の模式的な一部断面図を示すように、実施例 7 の配線構造は、基体 1 0 上の絶縁層 1 2 に形成された溝部 1 4、溝部 1 4 内に形成された多層の金属配線層 5 0 から成る。金属配線層 5 0 は、下から密着層 5 2、Cu 層 5 4 及び Ag 層 5 6 から構成されている。また、密着層 5 2 は、下から Ti 層 5 2 A / TiN 層 5 2 B の 2 層構造である。

【 0 0 8 9 】 実施例 7 の配線形成方法は、(イ) 基体 1 0 上に絶縁層 1 2 を形成した後、絶縁層 1 2 に溝部 1 4 を形成する工程と、(ロ) 溝部 1 4 を含む絶縁層 1 2 上に、下から密着層 5 2、Cu 層 5 4 及び Ag 層 5 6 から成る多層の金属配線層 5 0 を形成する工程と、(ハ) 絶縁層 1 2 上の金属配線層 5 0 を除去し、溝部 1 4 内に金属配線層を残す工程から成る。

【 0 0 9 0 】 密着層 5 2、Cu 層 5 4 及び Ag 層 5 6 の形成はスパッタ法にて行う。また、(ハ) の工程における絶縁層 1 2 上の金属配線層 5 0 の除去は、金属配線層 5 0 のケミカルメカニカルポリッシュ工程から成る。SiO<sub>2</sub> から成る絶縁層 1 2 をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する金属配線層 5 0 と絶縁層 1 2 の選択比を無限大まで設定することが可能となる。

【 0 0 9 1 】 以下、半導体装置等の模式的な一部断面図である図 1 3 を参照して、実施例 7 の配線形成方法を具体的に説明する。

【 0 0 9 2 】 [ 工程 - 7 0 0 ] 例えば半導体基板から成る基体 1 0 上に SiO<sub>2</sub> から成る絶縁層 1 2 を形成する。絶縁層 1 2 の形成条件を、例えば実施例 1 の [ 工程 - 1 0 0 ] と同様とすることができる。その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層 1 2 に溝部 1 4 を形成する。尚、溝部 1 4 は図 1 3 の紙面に垂直な方向に延びている。ドライエッチングの条件を、実施例 1 の [ 工程 - 1 1 0 ] と同様とすることができる。

【 0 0 9 3 】 [ 工程 - 7 1 0 ] 次に、下から Ti 層 5 2 A / TiN 層 5 2 B から成る密着層 5 2 を溝部 1 4 を含む絶縁層 1 2 上にスパッタ法にて形成する ( 図 1 3 の ( A ) 参照 )。密着層 5 2 を、例えば実施例 1 の [ 工程 - 1 2 0 ] と同様とすることができる。

【 0 0 9 4 】 [ 工程 - 7 2 0 ] その後、銅 ( Cu ) 層 5 4 をスパッタ法にて全面に形成する ( 図 1 3 の ( B ) 参照 )。Cu 層 5 4 の形成を、例えば以下のスパッタ条件にて行うことができる。

使用ガス : Ar = 1 0 0 sccm  
パワー : 1 0 kW

圧力 : 0. 4 7 Pa  
成膜温度 : 2 0 0 ° C  
膜厚 : 5 0 0 nm

【 0 0 9 5 】 [ 工程 - 7 3 0 ] その後、銀 ( Ag ) 層 5 6 をスパッタ法にて全面に形成する ( 図 1 3 の ( C ) 参照 )。Ag 層 5 6 の形成を、例えば以下の条件のスパッタ法にて行うことができる。

使用ガス : Ar = 1 0 0 sccm  
パワー : 1 0 kW  
圧力 : 0. 4 7 Pa  
成膜温度 : 2 0 0 ° C  
膜厚 : 1 0 0 nm

こうして Cu 層 5 4 の表面が Ag 層 5 6 で被覆される。

【 0 0 9 6 】 [ 工程 - 7 4 0 ] 次に、ケミカルメカニカルポリッシュ法によって絶縁層 1 2 上の Ag 層 5 6、Cu 層 5 4 及び密着層 5 2 を化学的及び機械的に研磨して除去し、溝部 1 4 内に Ag 層 5 6、Cu 層 5 4 及び密着層 5 2 を残し、金属配線層 5 0 から成る配線を形成する ( 図 1 2 参照 )。ケミカルメカニカルポリッシュには、図 4 に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、例えば以下のとおりとすることができる。

研磨プレート回転数 : 3 7 rpm  
基板保持台回転数 : 1 7 rpm  
研磨圧力 : 5. 5 × 1 0<sup>8</sup> Pa  
パッド温度 : 4 0 ° C

Ag 層 5 6 のケミカルメカニカルポリッシュ法による除去には I<sub>2</sub> + K I の混合水溶液を用いる。また、Cu 層 5 4 及び密着層 5 2 のケミカルメカニカルポリッシュ法による除去には K<sub>4</sub>Fe ( CN )<sub>6</sub> + H<sub>2</sub>O を用いる。

【 0 0 9 7 】 従来 SiO<sub>2</sub> を研磨する場合はスラリー ( SiO<sub>2</sub> 系の研磨剤 + KOH + 水 ) を用いるが、スラリーで SiO<sub>2</sub> を研磨する際、スラリーが研磨すべき面内に均一に分布しないため、研磨し過ぎ等により基板内の研磨面の平坦化にばらつきが生じるという問題がある。Ag 層 5 6、Cu 層 5 4 及び密着層 5 2 を研磨する場合、スラリーを必要とせず、I<sub>2</sub> + K I の混合水溶液、及び K<sub>4</sub>Fe ( CN )<sub>6</sub> 水溶液で研磨することで、Ag 層 5 6、Cu 層 5 4 及び密着層 5 2 のみを除去することが可能であり、基板内の研磨面の平坦化にばらつきも少ないという利点を有する。

【 0 0 9 8 】 これによって、平坦な絶縁層 1 2 に埋め込まれた金属配線層 5 0 から成る配線が形成される。実施例 7 においては、従来の配線形成方法のように金属配線層のレジストパターニング処理及びドライエッチング処理が不要となり、レジストパターニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。

【 0 0 9 9 】 ( 実施例 8 ) 実施例 7 では、絶縁層 1 2 上

のAg層56、Cu層54及び密着層52から成る金属配線層50の除去をケミカルメカニカルポリッシュ法にて行った。実施例2においては、その代わりに、ドライエッチングによるエッチバック法にて金属配線層50を除去する。尚、その他の工程は実施例7と同様であり、詳細な説明は省略する。

【0100】〔金属配線層50のエッチング工程〕溝部14を含む絶縁層12上に形成されたAg層56、Cu層54及び密着層52を、例えば以下の条件のドライエッチング法にてエッチバックし、溝部14内に密着層52、Cu層54及びAg層56から成る金属配線層50を残す。Ag層56のエッチング

使用ガス :  $\text{NO}_2/\text{O}_2=20/20\text{ sccm}$   
マイクロ波パワー : 850W  
RFパワー : 10W  
圧力 : 1.3Pa  
基板加熱温度 :  $100^\circ\text{C}$   
Cu層54及び密着層52のエッチング  
使用ガス :  $\text{O}_2/\text{Cl}_2=10/70\text{ sccm}$   
マイクロ波パワー : 1000W  
RFパワー : 300W  
圧力 : 0.5Pa  
基板加熱温度 :  $300^\circ\text{C}$

【0101】（実施例9）実施例9においては、実施例7の〔工程-710〕と〔工程-720〕との間に、溝部14の側壁にSiNから成るサイドウォール26を形成する工程を更に含む。尚、その他の工程は実施例7と同様であり、詳細な説明は省略する。以下、実施例9のサイドウォール26の形成工程を、図14を参照して説明する。サイドウォール26を形成することによって、絶縁層12による密着層52及びCu層54の酸化を防止することができる。

【0102】〔サイドウォール26の形成工程〕溝部14内を含む絶縁層12上の全面にプラズマCVD法にてSiN層26Aを堆積させる（図14の（A）参照）。次に、SiN層26Aを全面エッチバックする（図14の（B）参照）。SiN層26Aの形成条件及びエッチバックの条件を、例えば実施例3と同様とすることができる。これによって、溝部14の側壁にサイドウォール26が形成される。以降、実施例7の〔工程-720〕～〔工程-740〕を経て、図14の（C）に示す配線構造を形成することができる。

【0103】（実施例10）実施例9においてはSiNから成るサイドウォール26を溝部14の側壁に形成した。これに対して、実施例10においてはAg（銀）からサイドウォールを形成する。尚、その他の工程は実施例7と同様であり、詳細な説明は省略する。以下、実施例10のサイドウォールの形成工程を説明する。Agから成るサイドウォールを形成することによって、絶縁層12による密着層52及びCu層54の酸化を防止する

ことができる。

【0104】〔Agから成るサイドウォールの形成工程〕溝部14内を含む絶縁層12上の全面にスパッタ法にてAg層を堆積させる。次に、Ag層を全面エッチバックする。Ag層の形成条件及びエッチバックの条件を、以下に例示する。

Ag層形成条件

使用ガス :  $\text{Ar}=100\text{ sccm}$   
パワー : 4kW  
圧力 : 0.47Pa  
成膜温度 :  $200^\circ\text{C}$   
膜厚 : 100nm

Ag層エッチバック条件

使用ガス :  $\text{NO}_2/\text{O}_2=20/20\text{ sccm}$   
マイクロ波パワー : 850W  
RFパワー : 10W  
圧力 : 1.3Pa  
基板加熱温度 :  $100^\circ\text{C}$

こうして、図14に示したと同様のサイドウォールを溝部14の側壁に形成することができる。以降、実施例7の〔工程-720〕～〔工程-740〕を経て、図14の（C）に示したと同様の配線構造を形成することができる。

【0105】（実施例11）図15に模式的な一部断面図を示す実施例11の配線構造は、実施例7と若干異なり、半導体基板から成る基体10上の第1の絶縁層12Aに形成された開口部14Aと、第1の絶縁層12A上に形成された第2の絶縁層12Bに形成された溝部14Bと、開口部14A及び溝部14Bに埋め込まれた密着層52、Cu層54及びAg層56から成る金属配線層50から構成されている。この場合、開口部14Aの側壁及び溝部14Bの側壁にSiNから成るサイドウォール26を形成してもよい。また、開口部14Aを金属配線層50で埋め込むことによって、下層導体層（例えば、ソース・ドレイン領域36）と溝部14B内の配線58とが電気的に接続される。

【0106】実施例11の配線形成方法は、実施例7と若干異なり、予め半導体基板から成る基体10上の第1の絶縁層12Aに開口部14Aを、また、第1の絶縁層12A上に形成された第2の絶縁層12Bに溝部14Bを形成した後、密着層52、Cu層54及びAg層56から成る金属配線層50で開口部14A及び溝部14Bを埋め込み配線構造を形成する。第2の絶縁層12B上の金属配線層50はケミカルメカニカルポリッシュ法にて除去される。以下、半導体装置等の模式的な一部断面図である図16を参照して、実施例11の配線形成方法を説明する。

【0107】〔工程-1100〕Si（100）の半導体基板から成る基体10上に、通常の方法で素子分離領域30及びゲート領域32を形成する。次いで、LDD

イオン注入を行った後、ゲートサイドウォール34を形成し、ソース・ドレイン領域形成のために、不純物イオン注入を行う。

【0108】【工程-1110】その後、 $\text{SiO}_2$ 及びBPSGの2層から成る第1の絶縁層12Aを、例えばCVD法にて全面に形成し、リフロー処理を行い、第1の絶縁層12Aの平坦化を行う。

【0109】【工程-1120】次いで、第1の絶縁層12A上に、 $\text{SiO}_2$ から成る第2の絶縁層12Bを形成する。

【0110】【工程-1130】その後、第2の絶縁層12Bに溝部14Bを形成する。

【0111】【工程-1140】更に、第1の絶縁層12Aに開口部14Aを形成する。次いで、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。

【0112】以上の工程は、実施例4の【工程-400】～【工程-440】と同様とすることができる。

【0113】【工程-1150】次いで、実施例4の【工程-450】と同様に、 $\text{SiN}$ から成るサイドウォール26を開口部14A及び溝部14Bの側壁に形成してもよい。以上の工程によって、図16の(A)に示す構造が形成される。

【0114】【工程-1160】次に、下から $\text{Ti}$ 層/ $\text{TiN}$ 層から成る密着層52を開口部14A及び溝部14Bを含む第2の絶縁層12B上にスパッタ法にて形成する。この工程は、実施例1の【工程-120】と同様とすることができる。

【0115】【工程-1170】その後、実施例7の【工程-720】と同様に、 $\text{Cu}$ 層54をスパッタ法にて全面に形成する。次いで、実施例7の【工程-730】と同様に、 $\text{Ag}$ 層56をスパッタ法にて全面に形成する(図16の(B)参照)。

【0116】【工程-1180】その後、実施例7の【工程-740】と同様に、ケミカルメカニカルポリッシュ法によって第2の絶縁層12B上の $\text{Ag}$ 層56、 $\text{Cu}$ 層54及び密着層52を化学的及び機械的に研磨して除去し、溝部14B内及び開口部14A内に $\text{Ag}$ 層56、 $\text{Cu}$ 層54及び密着層52を残し、金属配線層50から成る接続孔及び配線を形成する(図15参照)。即ち、開口部14A内に金属配線層50が埋め込まれた接続孔58A(例えば、所謂コンタクトホール)が形成される。また、溝部14Bに金属配線層50が埋め込まれた配線58が形成される。

【0117】尚、 $\text{Ag}$ 層56、 $\text{Cu}$ 層54及び密着層52から成る金属配線層50をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例8と同様にドライエッチング法にてエッチバックすることで除去することもできる。

【0118】(実施例12) 実施例12は、実施例11

の変形である。実施例12の配線構造は実施例11と同様であるが、配線形成方法が実施例11と相違する。即ち、第1の絶縁層12Aに設けられた開口部14Aを $\text{Cu}$ から成る金属配線材料で埋め込み接続孔58Aを完成させた後、その上に第2の絶縁層12Bを堆積させ、かかる第2の絶縁層12Bに溝部14Bを形成する点が実施例11と相違する。実施例12においては、実施例11の【工程-1100】、【工程-1110】及び【工程-1140】は同様の工程であり、その他の工程が異なる。以下、図17を参照して、実施例12の方法を説明する。

【0119】

【工程-1200】～【工程-1220】 $\text{Si}$ (100)の半導体基板から成る基体10上に、通常の方法で素子分離領域30及びゲート領域32を形成する。次いで、 $\text{LDD}$ イオン注入を行った後、ゲートサイドウォール34を形成し、ソース・ドレイン領域形成のために、不純物イオン注入を行う。その後、 $\text{SiO}_2$ 及びBPSGの2層から成る第1の絶縁層12Aを、例えばCVD法にて全面に形成し、リフロー処理を行い、第1の絶縁層12Aの平坦化を行う。次いで、第1の絶縁層12Aに、レジストパターニング後ドライエッチングにて開口部14Aを形成し、開口部内にイオン注入を行うことにより、接合領域を形成させた後、活性化アニールを行う。これらの工程は、実施例4の【工程-1100】、【工程-1110】及び【工程-1140】と同様とすることができる。次いで、 $\text{SiN}$ から成るサイドウォール(図示せず)を開口部14Aの側壁に形成してもよい。

【0120】【工程-1230】

【工程-1220】の後、実施例7の【工程-710】と同様の方法で、下から $\text{Ti}$ / $\text{TiN}$ から成る第1の密着層52Aを全面に形成する。次いで、実施例7の【工程-720】と同様の方法で、第1の $\text{Cu}$ 層54Aをスパッタ法にて全面に成膜し、第1の密着層52Aと第1の $\text{Cu}$ 層54Aから成る第1の金属配線層を形成する。

【0121】【工程-1240】その後、ケミカルメカニカルポリッシュ法にて第1の絶縁層12A上の第1の金属配線層を除去し、開口部14A内のみに第1の金属配線層54A、52Aを残す(図17の(A)参照)。ケミカルメカニカルポリッシュの条件は、実施例7の【工程-740】の $\text{Cu}$ 層のケミカルメカニカルポリッシュと同様とすることができる。これによって、開口部14Aに第1の金属配線層が埋め込まれた所謂コンタクトホール58Aが形成される。ケミカルメカニカルポリッシュ法の代わりに、実施例8と同様に、ドライエッチング法によるエッチバックにて開口部14A内のみに第1の金属配線層54A、52Aを残してもよい。

【0122】【工程-1250】次いで、全面に $\text{SiO}_2$ から成る第2の絶縁層12Bを形成する。第2の絶縁

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層 1 2 B を、例えば実施例 1 1 の【工程-1 1 2 0】と同様の条件で形成することができる。その後、実施例 1 1 の【工程-1 1 3 0】と同様に、フォトリソグラフィ技術及びドライエッチング技術によって、第 2 の絶縁層 1 2 B に溝部 1 4 B を形成する。その後、必要に応じて、実施例 1 1 の【工程-1 1 5 0】と同様に、全面にプラズマ CVD 法にて SiN 層を形成し、次いで、SiN 層を全面エッチバックし、これによって、溝部 1 4 B の側壁に SiN から成るサイドウォール（図示せず）を形成してもよい。

【0 1 2 3】【工程-1 2 6 0】次に、実施例 7 の【工程-7 1 0】と同様の方法で、厚さ 3 0 n m の Ti から成る第 2 の密着層 5 2 B を溝部 1 4 B を含む第 2 の絶縁層 1 2 B 上にスパッタ法にて形成した後、実施例 7 の【工程-7 3 0】と同様の方法で、第 2 の Cu 層 5 4 B をスパッタ法にて全面に成膜し、更に、その上に Ag 層 5 6 をスパッタ法にて成膜することによって、第 2 の密着層 5 2 B、第 2 の Cu 層 5 4 B 及び Ag 層 5 6 から成る第 2 の金属配線層を形成する。

【0 1 2 4】【工程-1 2 7 0】次いで、ケミカルメカニカルポリッシュ法によって第 2 の絶縁層 1 2 B 上の第 2 の金属配線層 5 6、5 4 B、5 2 B を除去し、溝部 1 4 B 内に Ag 層 5 6、第 2 の Cu 層 5 4 B 及び第 2 の密着層 5 2 B を残し、配線 5 8 を形成する（図 1 8 の（B）参照）。ケミカルメカニカルポリッシュの条件は、実施例 7 の【工程-7 4 0】と同様とすることができる。

【0 1 2 5】尚、ケミカルメカニカルポリッシュ法によって第 2 の絶縁層 1 2 B 上の第 2 の金属配線層 5 6、5 4 B、5 2 B を除去する代わりに、実施例 8 と同様に、第 2 の金属配線層 5 6、5 4 B、5 2 B をドライエッチング法にてエッチバックし、これによって、溝部 1 4 B 内にのみ第 2 の金属配線層 5 6、5 4 B、5 2 B を残し、溝部 1 4 B 内に配線 5 8 を形成することもできる。

【0 1 2 6】（実施例 1 3）実施例 7 ～実施例 1 2 においては、半導体装置の配線構造を本発明の第 2 の態様に係る配線形成方法にて形成した。これに対して、実施例 1 3 ～実施例 1 5 における半導体装置の配線構造は、本発明の第 3 の態様に係る配線形成方法にて形成する。

【0 1 2 7】実施例 1 3 の半導体装置の配線形成方法は、（イ）基体 1 0 上に絶縁層 1 2 を形成した後、絶縁層 1 2 に溝部 1 4 を形成する工程と、（ロ）溝部 1 4 を含む絶縁層 1 2 上に、下から密着層 5 2 及び Cu 層 5 4 から成る多層の第 1 の金属配線層 5 0 A を形成する工程と、（ハ）絶縁層 1 2 上の第 1 の金属配線層 5 0 A を除去し、溝部 1 4 内に第 1 の金属配線層 5 0 A を残す工程と、（ニ）絶縁層 1 2 上及び第 1 の金属配線層 5 0 A 上に、Ag 層から成る第 2 の金属配線層 5 0 B を形成する工程と、（ホ）絶縁層 1 2 上の第 2 の金属配線層 5 0 B を除去し、溝部 1 4 内に第 2 の金属配線層 5 0 B を残す

工程から成る。

【0 1 2 8】密着層 5 2、Cu 層 5 4 及び第 2 の金属配線層 5 0 B の形成はスパッタ法にて行う。また、（ハ）の工程における絶縁層 1 2 上の第 1 の金属配線層 5 0 A の除去、並びに（ホ）の工程における絶縁層 1 2 上の第 2 の金属配線層 5 0 B の除去は、金属配線層 5 0 のケミカルメカニカルポリッシュ工程から成る。SiO<sub>2</sub> から成る絶縁層 1 2 をストッパーとして機能させることにより、ケミカルメカニカルポリッシュに対する第 1 及び第 2 の金属配線層 5 0 A、5 0 B と絶縁層 1 2 の選択比を無限大まで設定することが可能となる。

【0 1 2 9】本発明の第 3 の態様に係る配線形成方法においては、本発明の第 2 の態様に係る配線形成方法よりも一層確実に Cu 層 5 4 を Ag 層から成る第 2 の金属配線層 5 0 B で被覆することができる。

【0 1 3 0】以下、半導体装置等の模式的な一部断面図である図 1 8 及び図 1 9 を参照して、実施例 1 3 の配線形成方法を具体的に説明する。

【0 1 3 1】【工程-1 3 0 0】例えば半導体基板から成る基体 1 0 上に SiO<sub>2</sub> から成る絶縁層 1 2 を形成する。絶縁層 1 2 の形成条件を、例えば実施例 1 の【工程-1 0 0】と同様とすることができる。その後、フォトリソグラフィ技術及びドライエッチング技術によって、絶縁層 1 2 に溝部 1 4 を形成する。尚、溝部 1 4 は図 1 8 の紙面に垂直な方向に延びている。ドライエッチングの条件を、実施例 1 の【工程-1 1 0】と同様とすることができる。

【0 1 3 2】【工程-1 3 1 0】次に、下から Ti 層 5 2 A / TiN 層 5 2 B から成る密着層 5 2 を溝部 1 4 を含む絶縁層 1 2 上にスパッタ法にて形成する。密着層 5 2 を、例えば実施例 1 の【工程-1 2 0】と同様とすることができる。

【0 1 3 3】【工程-1 3 2 0】その後、銅（Cu）層 5 4 をスパッタ法にて全面に形成する（図 1 8 の（A）参照）。Cu 層 5 4 の形成を、実施例 7 の【工程-7 2 0】と同様とすることができる。こうして、溝部 1 4 を含む絶縁層 1 2 上に、下から密着層 5 2 及び Cu 層 5 4 から成る多層の第 1 の金属配線層 5 0 A を形成することができる。

【0 1 3 4】【工程-1 3 3 0】次に、ケミカルメカニカルポリッシュ法によって絶縁層 1 2 上の Cu 層 5 4 及び密着層 5 2 を化学的及び機械的に研磨して除去し、溝部 1 4 内に Cu 層 5 4 及び密着層 5 2 から成る第 1 の金属配線層 5 0 A を残す（図 1 8 の（B）参照）。ケミカルメカニカルポリッシュには、図 4 に示す研磨装置を用いる。ケミカルメカニカルポリッシュの条件を、実施例 1 3 と同様とすることができる。Cu 層 5 4 及び密着層 5 2 のケミカルメカニカルポリッシュ法による除去には K<sub>4</sub>Fe(CN)<sub>6</sub> + H<sub>2</sub>O を用いる。

【0 1 3 5】【工程-1 3 4 0】その後、銀（Ag）層

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から成る第2の金属配線層50Bをスパッタ法にて全面に形成する(図19の(A)参照)。Ag層の形成を、実施例13の[工程-730]と同様とすることができる。こうして第1の金属配線層50Aの表面がAg層から成る第2の金属配線層50Bで被覆される。

【0136】[工程-1350] 次に、ケミカルメカニカルポリッシュ法によって絶縁層12上のAg層から成る第2の金属配線層50Bを化学的及び機械的に研磨して除去し、溝部14内にAg層から成る第2の金属配線層50Bを残し、第1及び第2の金属配線層50A、50Bから成る配線を形成する(図19の(B)参照)。ケミカルメカニカルポリッシュの条件は、実施例13と同様とすることができる。尚、Ag層のケミカルメカニカルポリッシュ法による除去には $H_2+KCl$ の混合水溶液を用いる。

【0137】実施例13においては、従来の配線形成方法のように金属配線層のレジストパターンニング処理及びドライエッチング処理が不要となり、レジストパターンニング時の光の散乱の問題、エッチングが不均一となる問題を回避することができる。また、配線上の絶縁膜の形成及びかかる絶縁膜の平坦化処理も不要である。また、第1の金属配線層50Aの表面は第2の金属配線層50Bによって一層確実に被覆されているので、第1の金属配線層50Aを構成するCu層54の酸化を防止することができる。

【0138】実施例13においては、第1の金属配線層50A及び第2の金属配線層50Bの除去を専らケミカルメカニカルポリッシュ法にて行ったが、実施例8と同様にドライエッチング法によるエッチバックにて除去することもできる。

【0139】また、実施例13にて説明した本発明の第3の態様に係る半導体装置の配線形成方法と、実施例9あるいは実施例10にて説明したサイドウォールの形成とを組み合わせることもできる。更には、実施例11あるいは実施例12におけるAg層56の代わりに、実施例13にて説明した配線形成方法を適用することもできる。

【0140】(実施例14) 実施例11におけるAg層56の代わりに、実施例13にて説明した配線形成方法を適用する場合の工程のフローのみを、以下に説明する。尚、第1及び/又は第2の金属配線層をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例8と同様にドライエッチング法にてエッチバックすることでも除去することもできる。

【0141】[工程-1400] 基体上への、素子分離領域、ゲート領域の形成。LDDイオン注入。ゲートサイドウォールの形成。ソース・ドレイン領域形成のための不純物イオン注入。

[工程-1410]  $SiO_2$ 及びBPSGの2層から成る第1の絶縁層の形成及びリフロー処理。

[工程-1420] 第1の絶縁層上への $SiO_2$ から成る第2の絶縁層の形成。

[工程-1430] 第2の絶縁層への溝部の形成。

[工程-1440] 第1の絶縁層への開口部の形成。

[工程-1450] Ti層/TiN層から成る密着層の開口部及び溝部を含む第2の絶縁層上へのスパッタ法による形成。

[工程-1460] 密着層上へのスパッタ法によるCu層の形成。

[工程-1470] ケミカルメカニカルポリッシュによる第2の絶縁層上のCu層の除去。

[工程-1470] 全面に、スパッタ法によるAg層から成る第2の金属配線層の形成。

[工程-1480] ケミカルメカニカルポリッシュ法による第2の絶縁層上の第2の金属配線層の除去。

【0142】(実施例15) 実施例12におけるAg層56の代わりに、実施例13にて説明した配線形成方法を適用する場合の工程のフローのみを、以下に説明する。尚、第1及び/又は第2の金属配線層をケミカルメカニカルポリッシュ法にて除去する代わりに、実施例8と同様にドライエッチング法にてエッチバックすることでも除去することもできる。

【0143】[工程-1500] 基体上への、素子分離領域、ゲート領域の形成。LDDイオン注入。ゲートサイドウォールの形成。ソース・ドレイン領域形成のための不純物イオン注入。

[工程-1510]  $SiO_2$ 及びBPSGの2層から成る第1の絶縁層の形成及びリフロー処理。

[工程-1520] 第1の絶縁層への開口部の形成。

[工程-1530] 第1の絶縁層上への第1の密着層及び第1のCu層から成る第1の金属配線層のスパッタ法による形成。

[工程-1540] ケミカルメカニカルポリッシュ法による第1の絶縁層上の第1の金属配線層の除去。これによって、開口部に第1の金属配線層が埋め込まれた所謂コンタクトホールを形成。

[工程-1550] 全面に、 $SiO_2$ から成る第2の絶縁層の形成。第2の絶縁層への溝部の形成。

[工程-1560] 第2の絶縁層上への第2の密着層及びCu層のスパッタ法による形成。

[工程-1570] ケミカルメカニカルポリッシュによる第2の絶縁層上のCu層及び第2の密着層の除去。

[工程-1580] 全面に、スパッタ法によるAg層から成る第2の金属配線層の形成。

[工程-1590] ケミカルメカニカルポリッシュ法による第2の絶縁層上の第2の金属配線層の除去。

【0144】以上、本発明を好ましい実施例に基づき説明したが、本発明はこれらの実施例に限定されるものではない。実施例にて用いた各種材料や条件は例示であり、適宜変更することができる。場合によっては、溝部



14, 14Bの代わりに開口部を形成することができる。

【0145】絶縁層は専らSiO<sub>2</sub>あるいはSiO<sub>2</sub>とBPSGの組み合わせから成るものとして説明したが、これらの代わりに、BPSG、PSG、BSG、AsSG、PbSG、SbSG、SOG、SiONあるいはSiN等の公知の絶縁材料、あるいはこれらの絶縁層を積層したものから構成することができる。

【0146】実施例1～実施例6においては、Ag層20の形成は、Ag<sub>2</sub>CO<sub>3</sub>を原料として用いた化学気相析出法にて行ったが、その代わりに、AgNO<sub>2</sub>、AgBr若しくはAgIを原料として用いた化学気相析出法にて行うことができる。これらの場合のCVD条件、及び図3に示したCVD装置において第1及び第2のヒーター206, 210によって配管204及びCVDチャンバ導入部208内を流れる原料ガスの加熱条件を以下に例示し、併せて反応式を示す。

【0147】原料：AgNO<sub>2</sub>  
原料源温度：150°C  
使用ガス：AgNO<sub>2</sub>/Ar/H<sub>2</sub>=10/25/1000sccm  
圧力：2.6×10<sup>3</sup>Pa  
基板加熱温度：450°C  
ガス加熱条件：140°C以上  
反応式： $2AgNO_2 + 7H_2 \rightarrow 2Ag + 2NH_3 \uparrow + 4H_2O \uparrow$

【0148】原料：AgBr  
原料源温度：450°C  
使用ガス：AgBr/Ar/H<sub>2</sub>=10/75/1000sccm  
圧力：2.6×10<sup>3</sup>Pa  
基板加熱温度：500°C  
ガス加熱条件：434°C以上  
パワー：500W（プラズマCVD）  
反応式： $2AgBr + H_2 \rightarrow 2Ag + 2HBr \uparrow$

【0149】原料：AgI  
原料源温度：560°C  
使用ガス：AgI/Ar/H<sub>2</sub>=10/100/1000sccm  
圧力：2.6×10<sup>3</sup>Pa  
基板加熱温度：600°C  
ガス加熱条件：552°C以上  
パワー：500W（プラズマCVD）  
反応式： $2AgI + H_2 \rightarrow 2Ag + 2HI \uparrow$

【0150】実施例7～実施例15において、Cu層及び/又はAg層をスパッタ法にて形成する代わりに、CVD法にて形成することができる。CVD法によるCu層の形成条件を以下に例示する。

使用ガス：Cu(HFA)<sub>2</sub>/H<sub>2</sub>=10/100

0sccm

圧力：2.6×10<sup>3</sup>Pa

基板加熱温度：350°C

パワー：500W

尚、HFAとは、ヘキサフルオロアセチルアセトネートの略である。

【0151】密着層を、Ti層/TiN層の代わりに、Ti層、あるいはTiN層から構成することもできる。この場合の、Ti層又はTiN層の形成条件は、実施例1の【工程-120】にて説明したTi層18A、TiN層18Bの形成条件と同様とすることができる。あるいは又、密着層を、下からAg層/Ti層の2層構造とすることもできる。この場合、Ag層を、以下の条件のスパッタ法にて形成することができる。また、Ti層の形成条件は、実施例1の【工程-120】にて説明したTi層18Aの形成条件と同様とすることができる。

Ag層のスパッタ条件

使用ガス：Ar=100sccm

パワー：4kW

圧力：0.47Pa

成膜温度：200°C

膜厚：50nm

【0152】密着層を構成するTiNの代わりに、TiONやTiWを用いることもできる。また、場合によっては、溝部の形成、サイドウォールの形成、密着層の形成の順序を変更して、溝部の形成、密着層の形成、サイドウォールの形成の順とすることもできる。また、Ti、TiN等の密着層を構成する金属層又は金属化合物層は、CVD等の成膜法で形成することができる。

【0153】基体としては、シリコン半導体基板、あるいはソース・ドレイン領域が形成された半導体基板の他にも、MgO基板、GaAs基板、超伝導トランジスタ基板、下層配線層が形成された絶縁層、接続孔（コンタクトホール、ビヤホール、スルーホール）を形成して電気的接続を形成する必要があるゲート電極等の各種素子部、薄膜トランジスタを作製するための各種基板上に形成されたシリコン層等を挙げることができる。

【0154】実施例6においては、所謂ブランケットタングステンCVD法を用いて開口部14A内にタングステンプラグを形成したが、代わりに、所謂タングステン選択CVD法にて開口部14A内にタングステンプラグを形成してもよい。この場合の条件を、例えば以下のとおりとすることができる。使用ガス：WF<sub>6</sub>/SiH<sub>4</sub>/H<sub>2</sub>/Ar=10/7/1000/10sccm

温度：260°C

圧力：26Pa

【0155】本発明は、MOS半導体装置以外の他の半導体装置（例えば、バイポーラトランジスタ、CCD）にも適用できる。

【0156】スパッタ法は、マグネトロンスパッタリング装置、DCスパッタリング装置、RFスパッタリング装置、ECRスパッタリング装置、また基板バイアスを印加するバイアスパッタリング装置等各種のスパッタリング装置にて行うことができる。

【0157】本発明の第1の態様に係る配線構造においてはAg層の下に、また、本発明の第2の態様に係る配線構造においてはCu層の下に、あるいは又、密着層の下に配線層若しくは接続孔に、Mo、Ti等の高融点金属、又は、TiW、ZrN、W、WC、TiC、その他 10 MoSi<sub>2</sub>、WSi<sub>2</sub>、TiSi<sub>2</sub>等のシリサイド等を単層若しくは各種組み合わせた多層膜を形成することができる。

【0158】

【発明の効果】本発明においては、配線を形成するためのフォトリソグラフィ技術及びドライエッチング技術による金属配線層のパターニング工程が不要である。従って、従来のフォトリソグラフィ技術における光の乱反射、あるいはドライエッチングにおけるエッチングの不 20 均一性やコロージョンの問題を回避することができる。

【0159】また、微細な配線を有する半導体装置の作製において、従来のように配線上に形成された絶縁膜の形成、あるいはかかる絶縁膜の研磨を行わずに、配線を含む絶縁層の完全なる平坦化が可能となる。従来のSiO<sub>2</sub>系絶縁膜は研磨における選択性が乏しいために研磨の制御性が乏しかったが、金属配線層の研磨は絶縁層に対する選択性が大きいので、研磨の制御性も格段に向上する。

【0160】更に、溝部又は開口部内のみに金属配線層を残すために、ケミカルメカニカルポリッシュ法あるいはドライエッチング法によるエッチバックを採用することによって、従来の技術を基本的にはそのまま用いることができ、半導体装置の製造コストが増加することもない。

【0161】尚、溝部又は開口部内にサイドウォールを形成することで、金属配線層の酸化を防止でき、しかも金属配線層によって溝部又は開口部を安定して埋め込むことができる。

【0162】本発明の第1の態様に係る配線構造及び配線形成方法においては、Al系合金より耐エレクトロマイグレーション性を有するAg層から配線構造を構成するので半導体素子の信頼性が従来より向上する。更に、AgはAl系合金より抵抗が低いので半導体素子の応答 40 スピードが期待できる。

【0163】本発明の第2の態様に係る配線構造、並びに第2及び第3の態様に係る配線形成方法においては、Al系合金より耐エレクトロマイグレーション性を有するCu層から金属配線層を構成するので半導体素子の信頼性が従来より向上する。また、Cu層の表面はAg層で被覆されているので、Cu層の酸化を防ぐと同時に、 50

Agの低抵抗性によって配線抵抗を低く保つことができる。従来、Cuは酸化等の問題でプロセス限定の必要があったが、酸素雰囲気等の熱処理等のプロセスを用いることが可能になる。

【0164】本発明の銀薄膜形成方法により、AgのCVDが可能となり、溝部や開口部へのAgの完全埋め込みが可能となる。

【0165】更には、本発明のCVD装置においては、CVDチャンバへのソース供給配管及びCVDチャンバの接続部を高い温度に保持できるので、安定して原料ガスを供給することができる。

【図面の簡単な説明】

【図1】実施例1の半導体装置の配線構造の模式的な図である。

【図2】実施例1の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図3】本発明のCVD装置の模式図である。

【図4】本発明の実施に適した研磨装置の模式図である。

【図5】実施例3のサイドウォール形成工程を説明するための半導体素子等の模式的な一部断面図である。

【図6】実施例4の半導体装置の配線構造の模式的な図である。

【図7】実施例4の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図8】図7に引き続き、実施例4の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図9】実施例5の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図10】図9に引き続き、実施例5の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図11】実施例6の配線形成方法の工程を説明するための半導体素子等の模式的な一部断面図である。

【図12】実施例7の半導体装置の配線構造の模式的な図である。

【図13】実施例7の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図14】実施例9のサイドウォール形成工程を説明するための半導体素子等の模式的な一部断面図である。

【図15】実施例11の半導体装置の配線構造の模式的な図である。

【図16】実施例11の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図17】実施例12の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図18】実施例13の配線形成方法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図19】図18に引き続き、実施例13の配線形成方



法の各工程を説明するための半導体素子等の模式的な一部断面図である。

【図20】従来の半導体素子の製造プロセス例における各工程を説明するための半導体装置等の模式的な一部断面図である。

【図21】図20に引き続き、従来の半導体素子の製造プロセス例における各工程を説明するための半導体装置等の模式的な一部断面図である。

【図22】従来の半導体素子の製造プロセスの別の例における各工程を説明するための半導体装置等の模式的な一部断面図である。

【図23】従来の半導体素子の製造プロセスにおける問題点を説明するための図である。

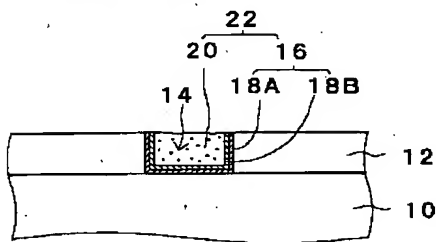
【符号の説明】

- 10 基体
- 12, 12A, 12B 絶縁層
- 14, 14B 溝部
- 14A 開口部
- 16, 16A, 16B 密着層
- 18A Ti層
- 18B TiN層
- 20 Ag層
- 22 金属配線層
- 24 配線
- 24A 接続孔

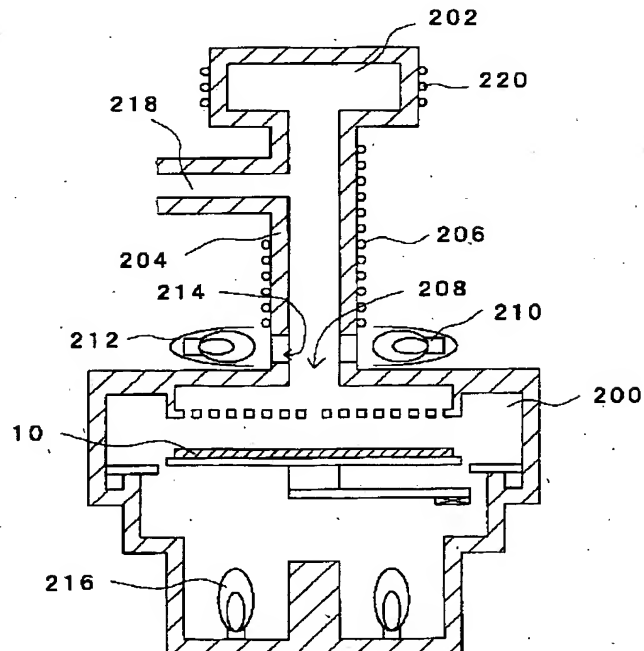
- 26A SiN層
- 26 サイドウォール
- 30 素子分離領域
- 32 ゲート領域
- 34 ゲートサイドウォール
- 36 ソース・ドレイン領域
- 40 バリア層
- 42 タングステン層
- 50 金属配線層
- 50A 第1の金属配線層
- 50B 第2の金属配線層
- 52, 52A, 52B 密着層
- 54, 54A, 54B Cu層
- 56 Ag層
- 58 配線
- 58A 接続孔
- 200 CVDチャンバ
- 202 原料源
- 204 配管
- 206 第1のヒーター
- 208 CVDチャンバ導入部
- 210 第2のヒーター
- 214 窓
- 216 ランプ加熱装置
- 218 不活性ガス導入部

【図1】

(実施例1の配線構造)

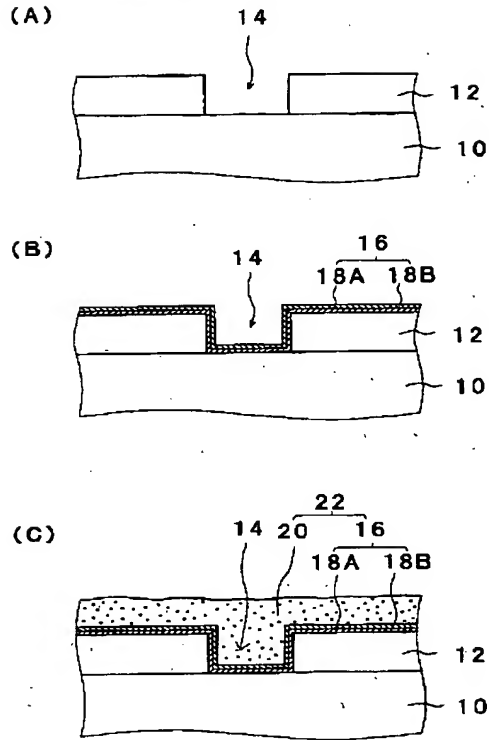


【図3】



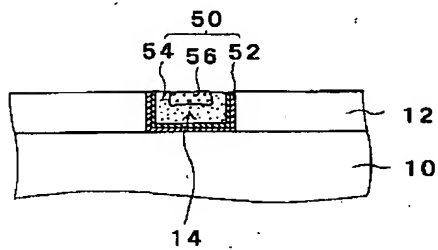
【図2】

(実施例1の配線形成方法)

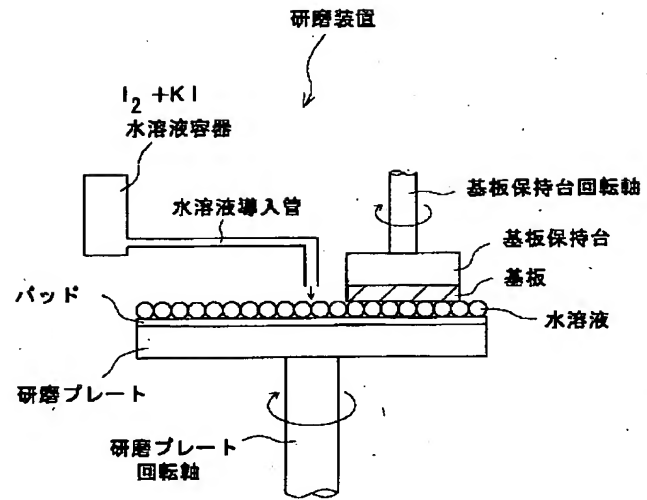


【図12】

(実施例7の配線構造)

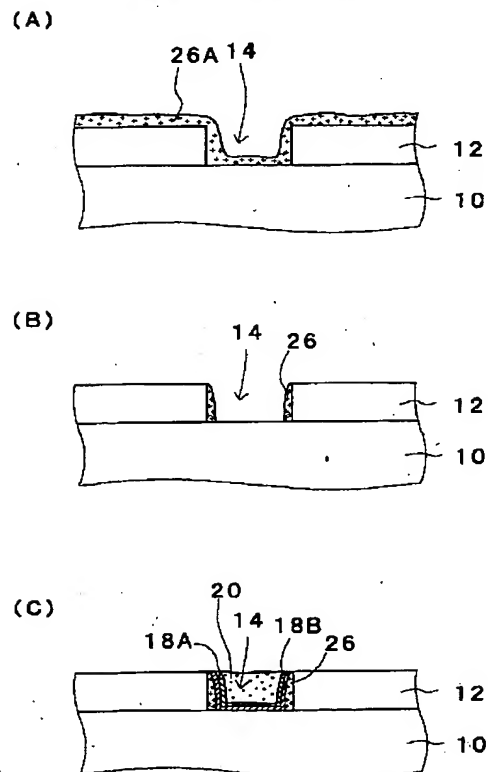


【図4】



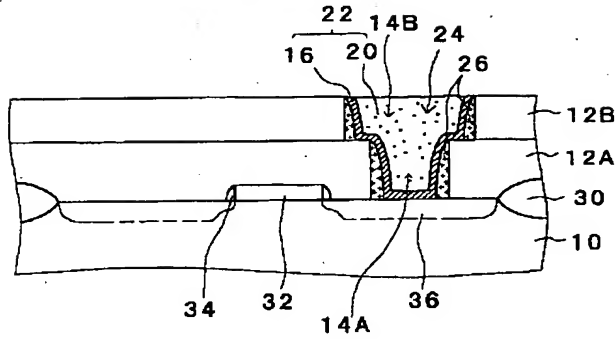
【図5】

(実施例3の配線形成方法)



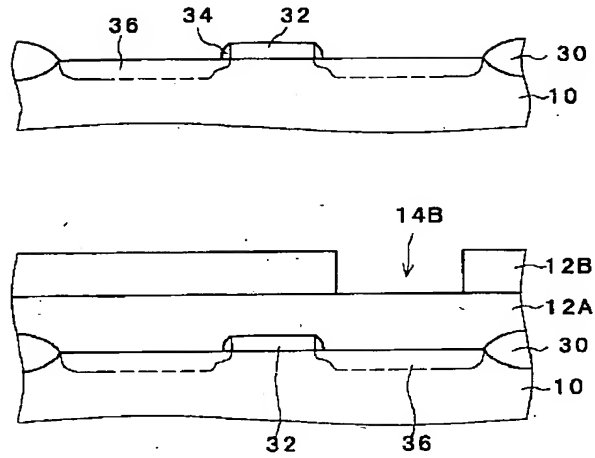
【図6】

(実施例4の配線構造)



【図7】

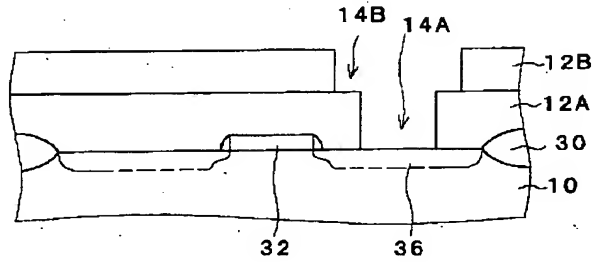
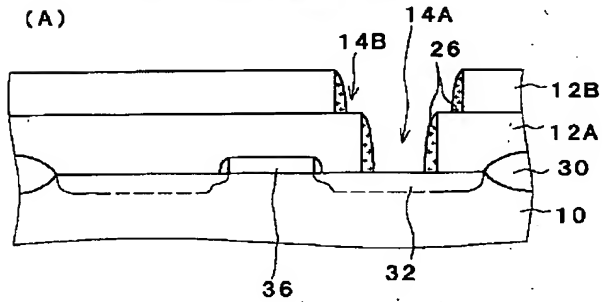
(実施例4の配線形成方法)



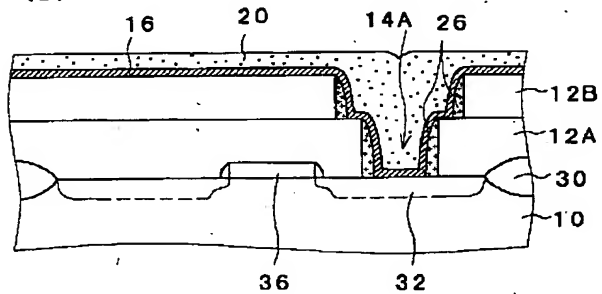
【図8】

(実施例4の配線形成方法) (続き)

(A)

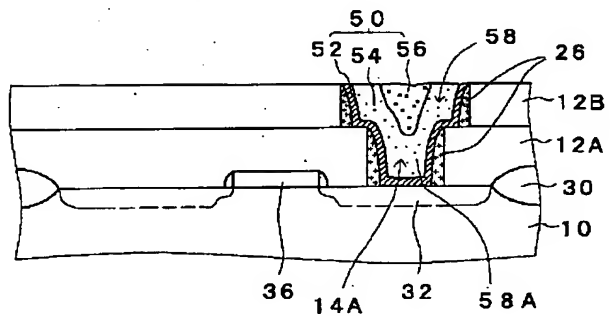


(B)



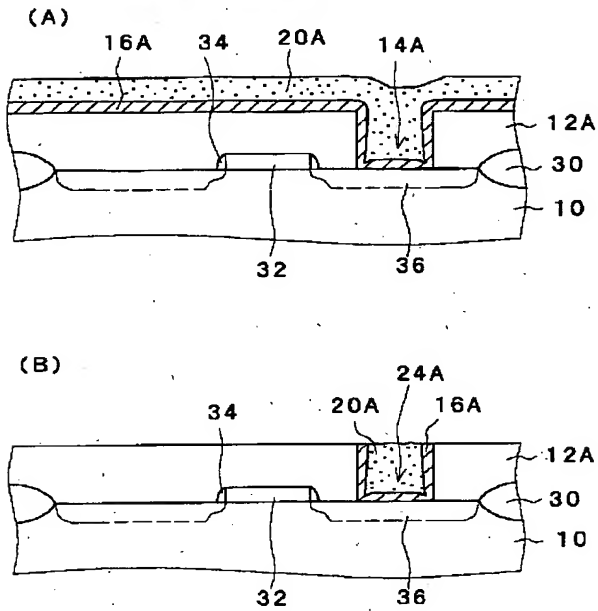
【図15】

(実施例11の配線構造)



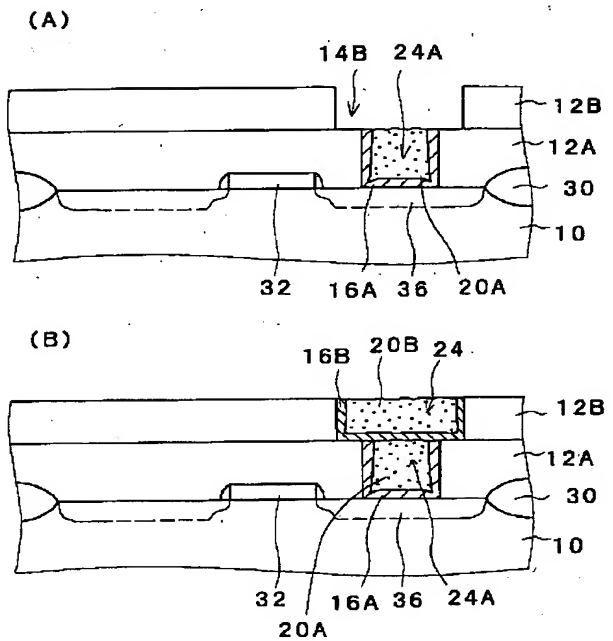
【図 9】

(実施例 5 の配線形成方法)



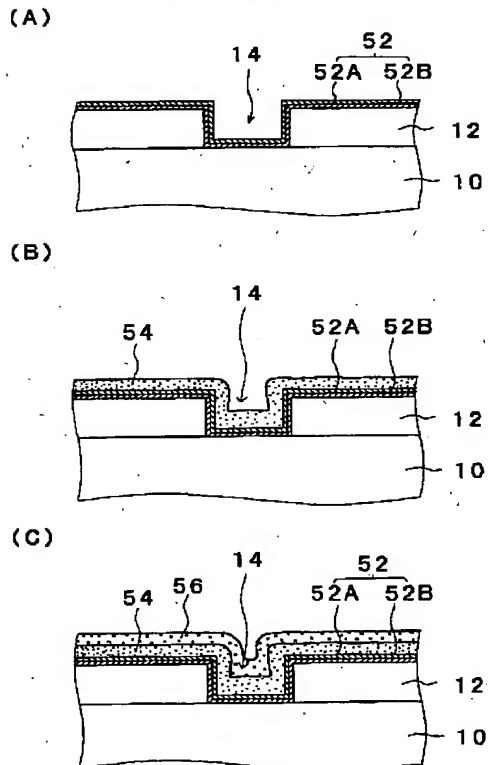
【図 10】

(実施例 5 の配線形成方法) (続き)



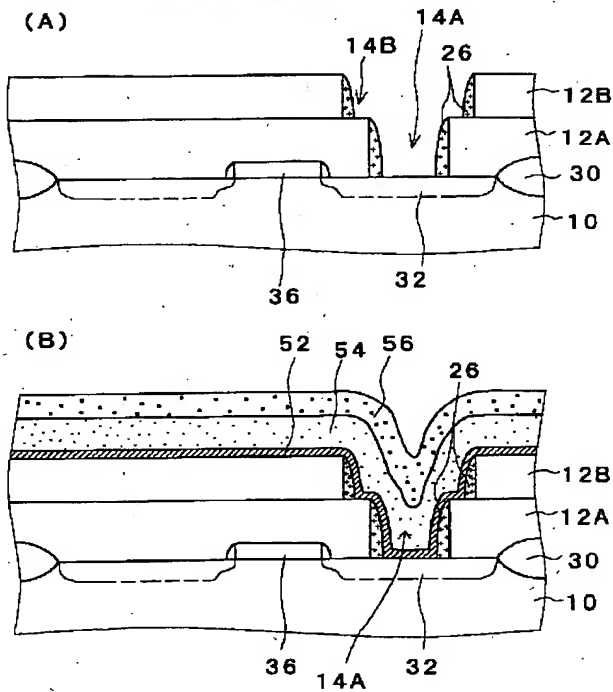
【図 13】

(実施例 7 の配線形成方法)

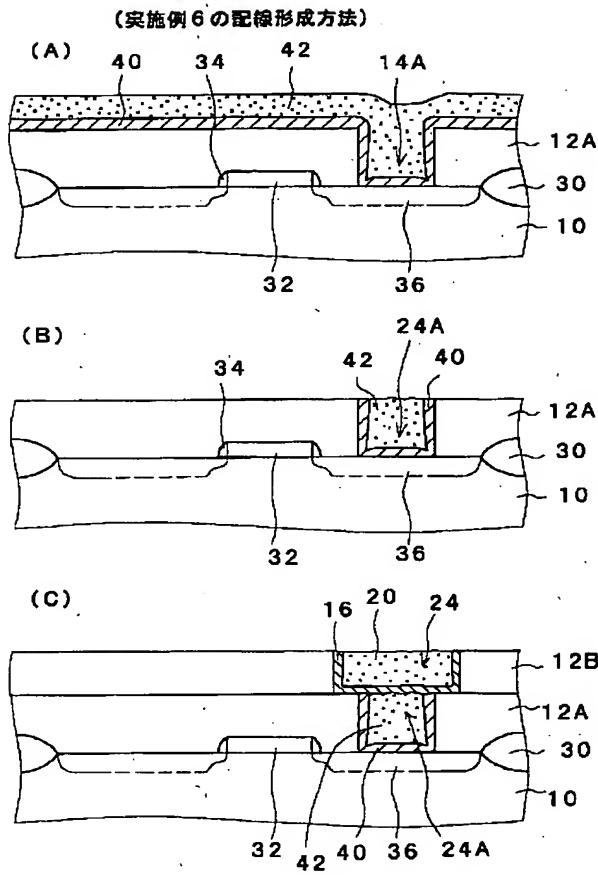


【図 16】

(実施例 11 の配線形成方法)

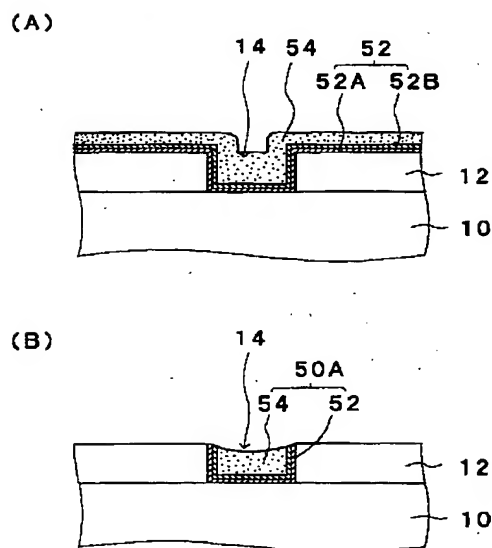


【図11】



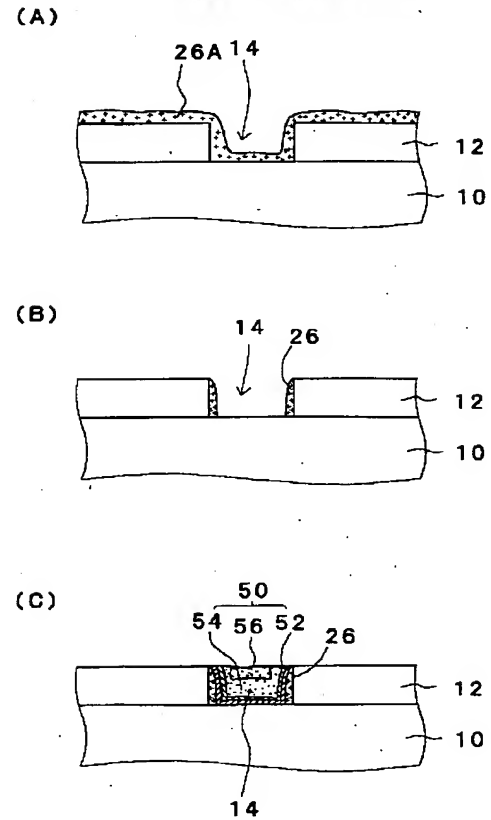
【図18】

(実施例13の配線形成方法)



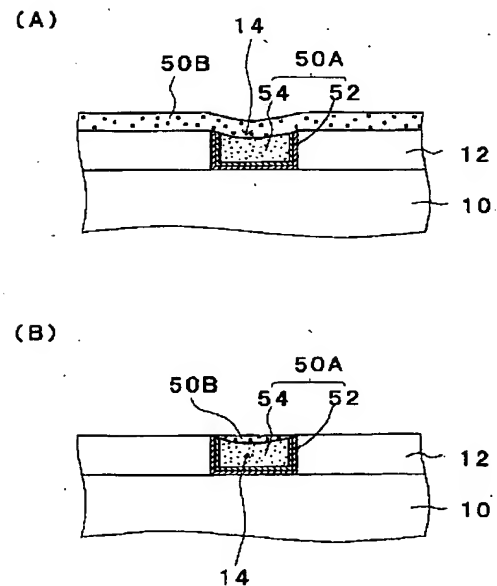
【図14】

(実施例9の配線形成方法)



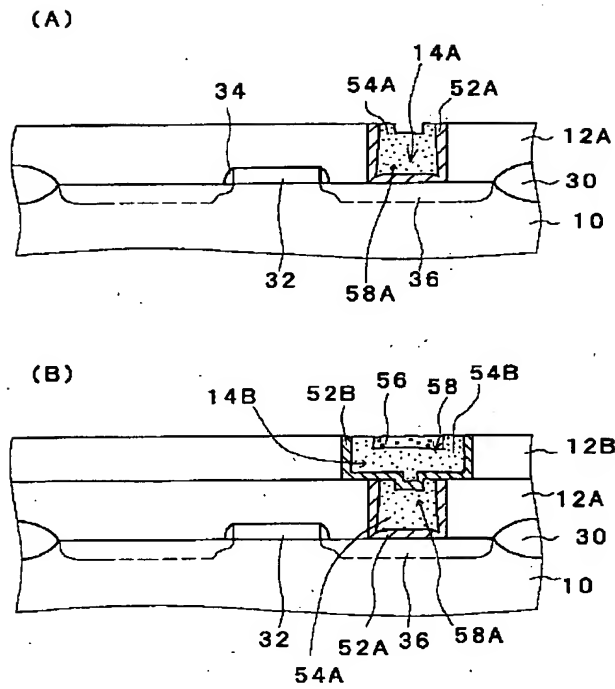
【図19】

(実施例13の配線形成方法) (続き)



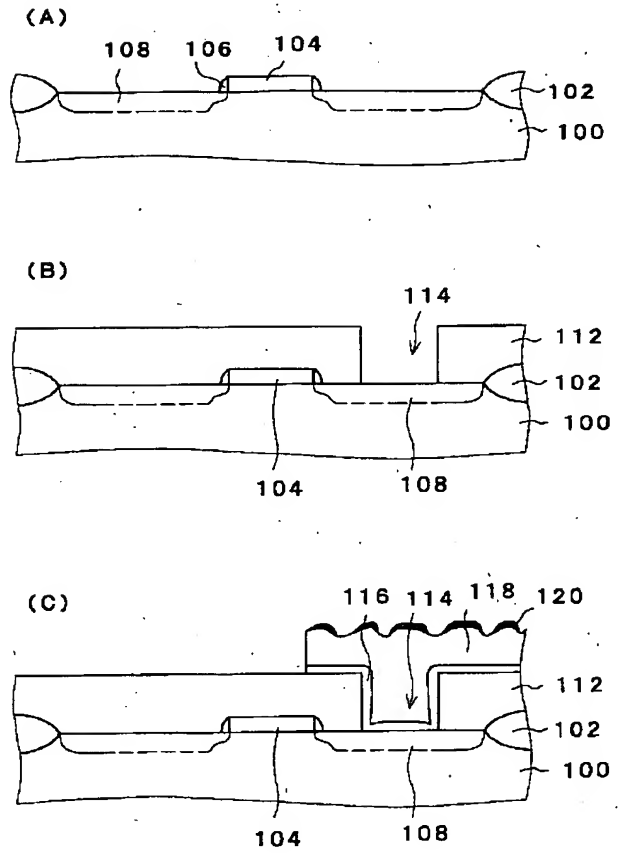
【図17】

(実施例12の配線形成方法)



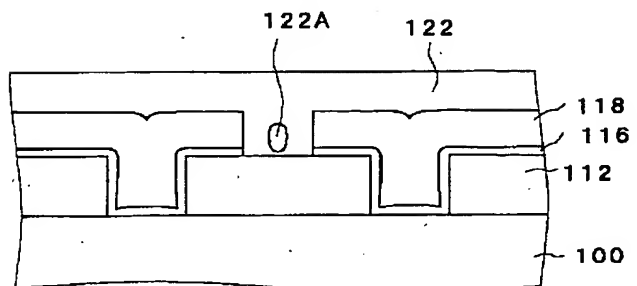
【図20】

(従来技術, その1)



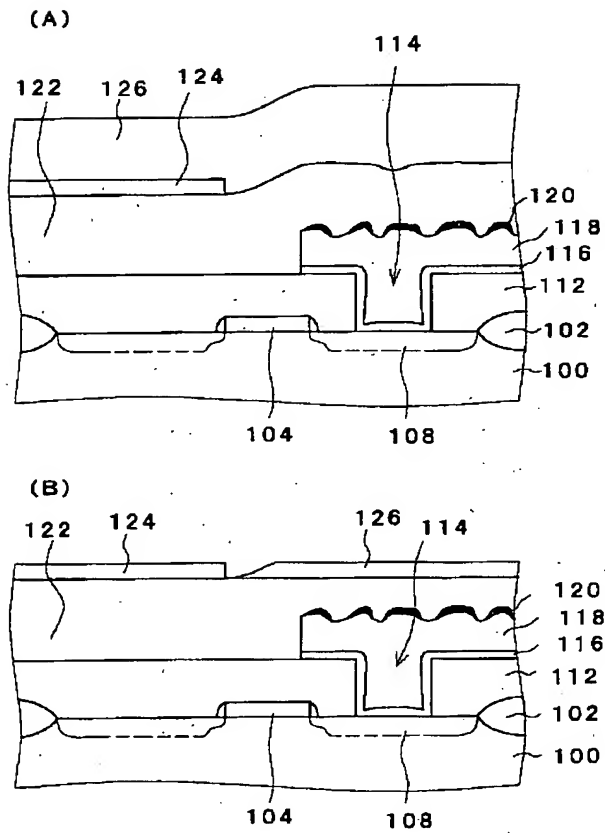
【図23】

(従来技術における問題点)



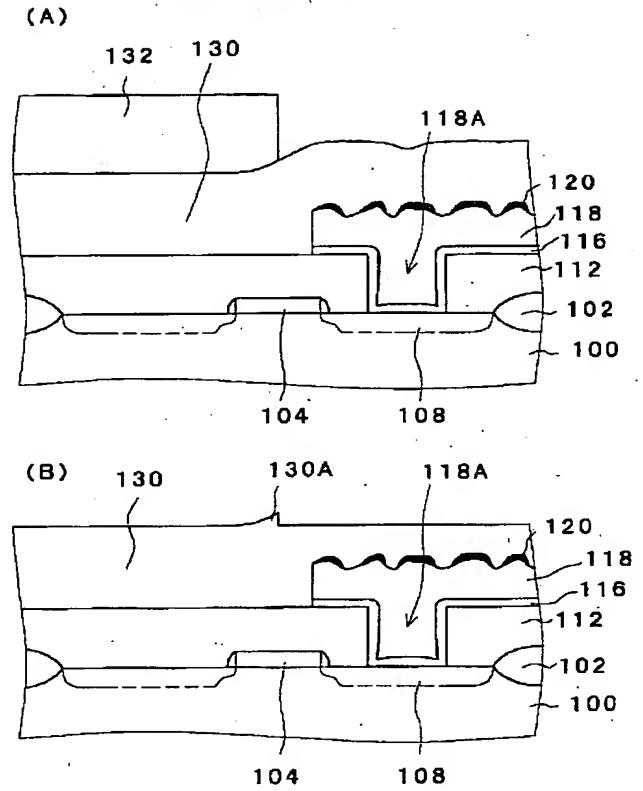
【図 21】

(従来技術, その1) (続き)



【図 22】

(従来技術, その2)



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